

FIG. 1

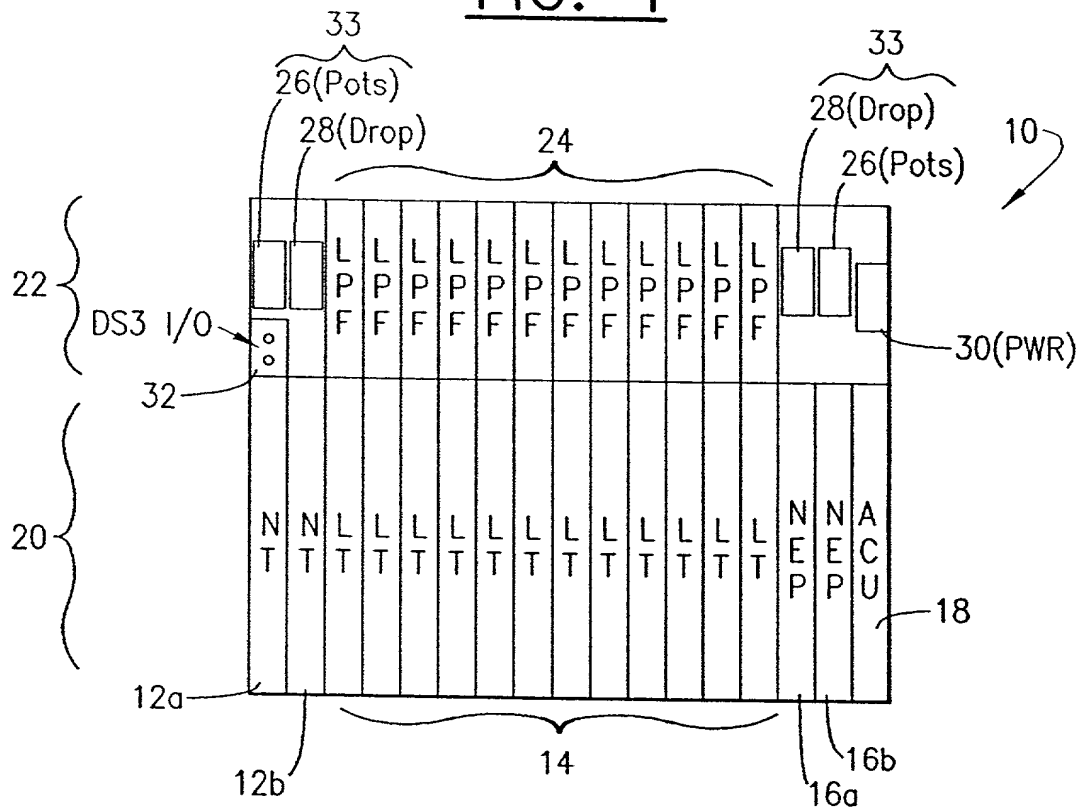


FIG. 2

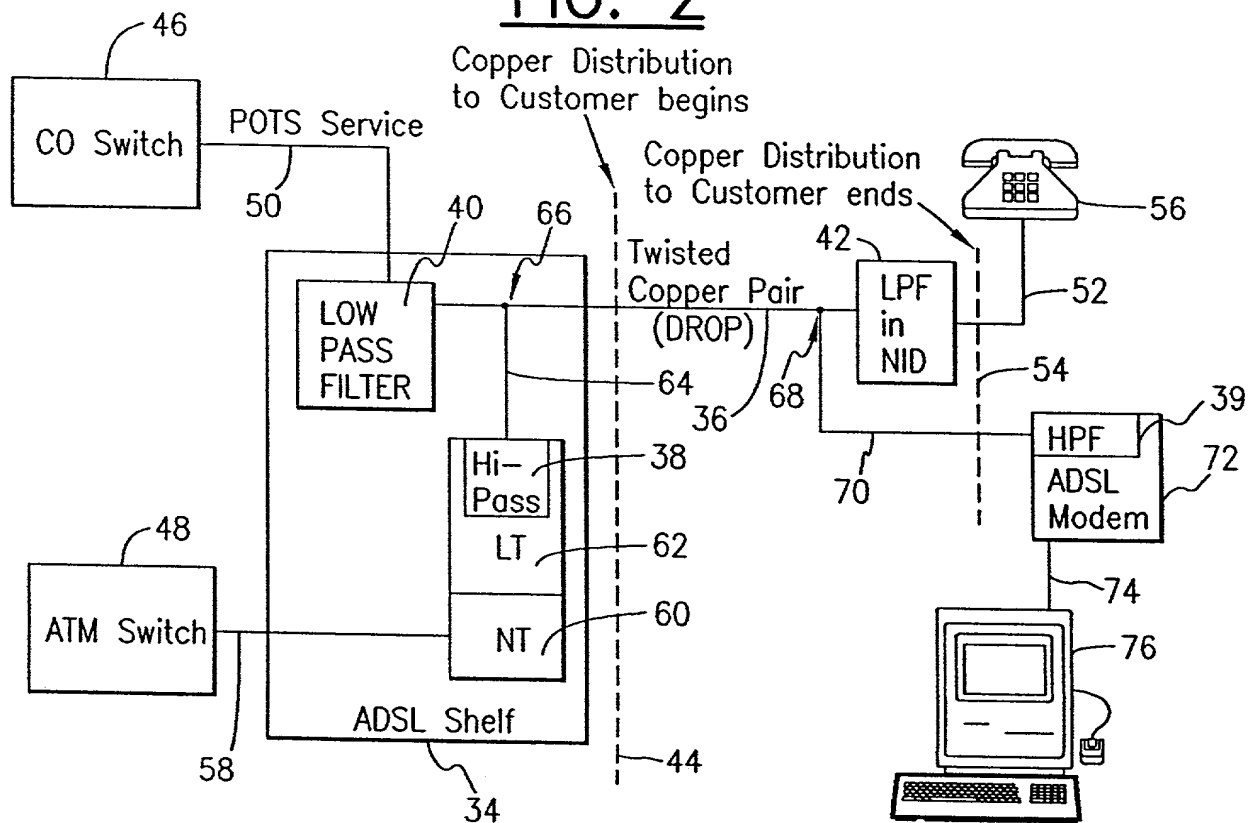


FIG. 1A

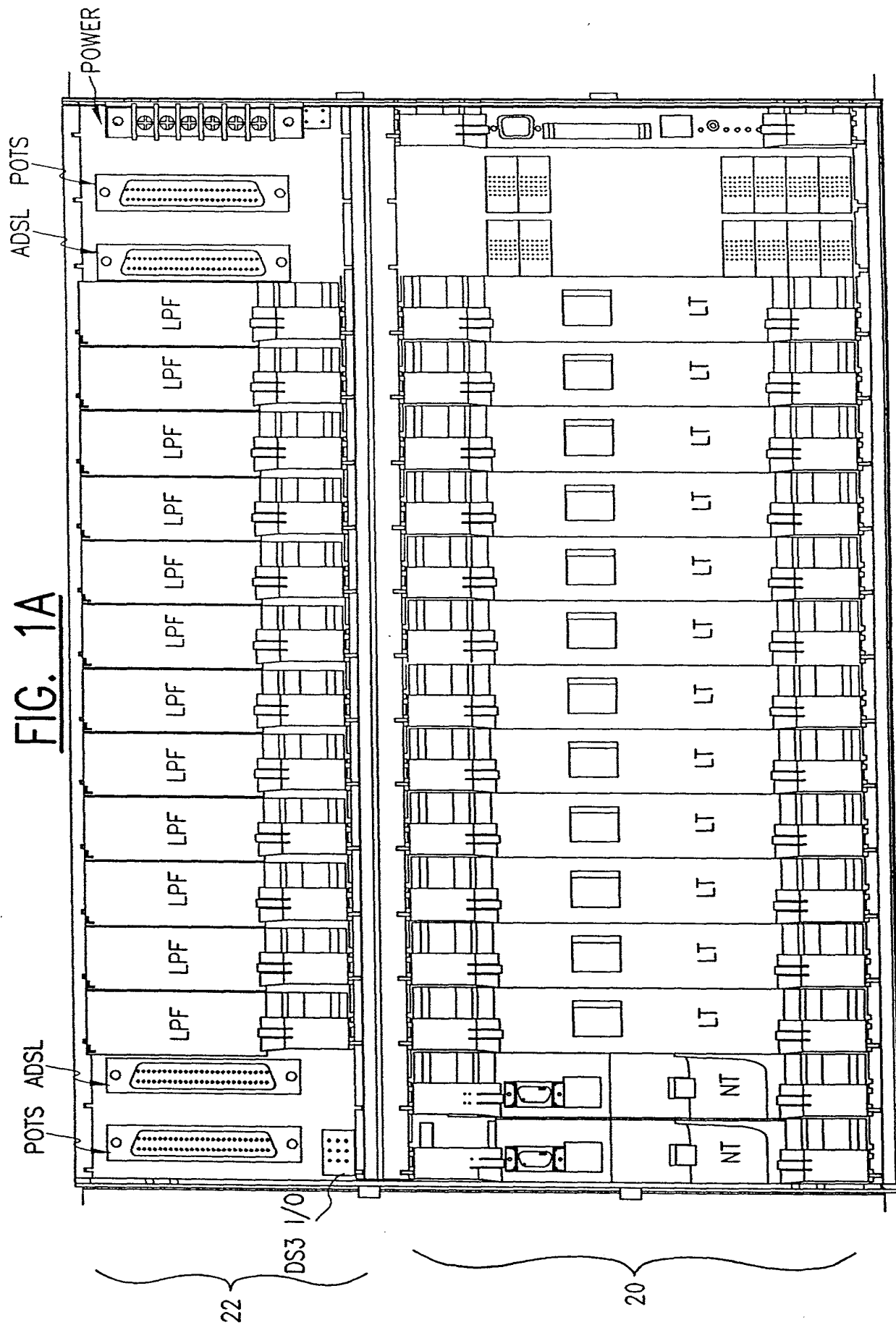


FIG. 1B

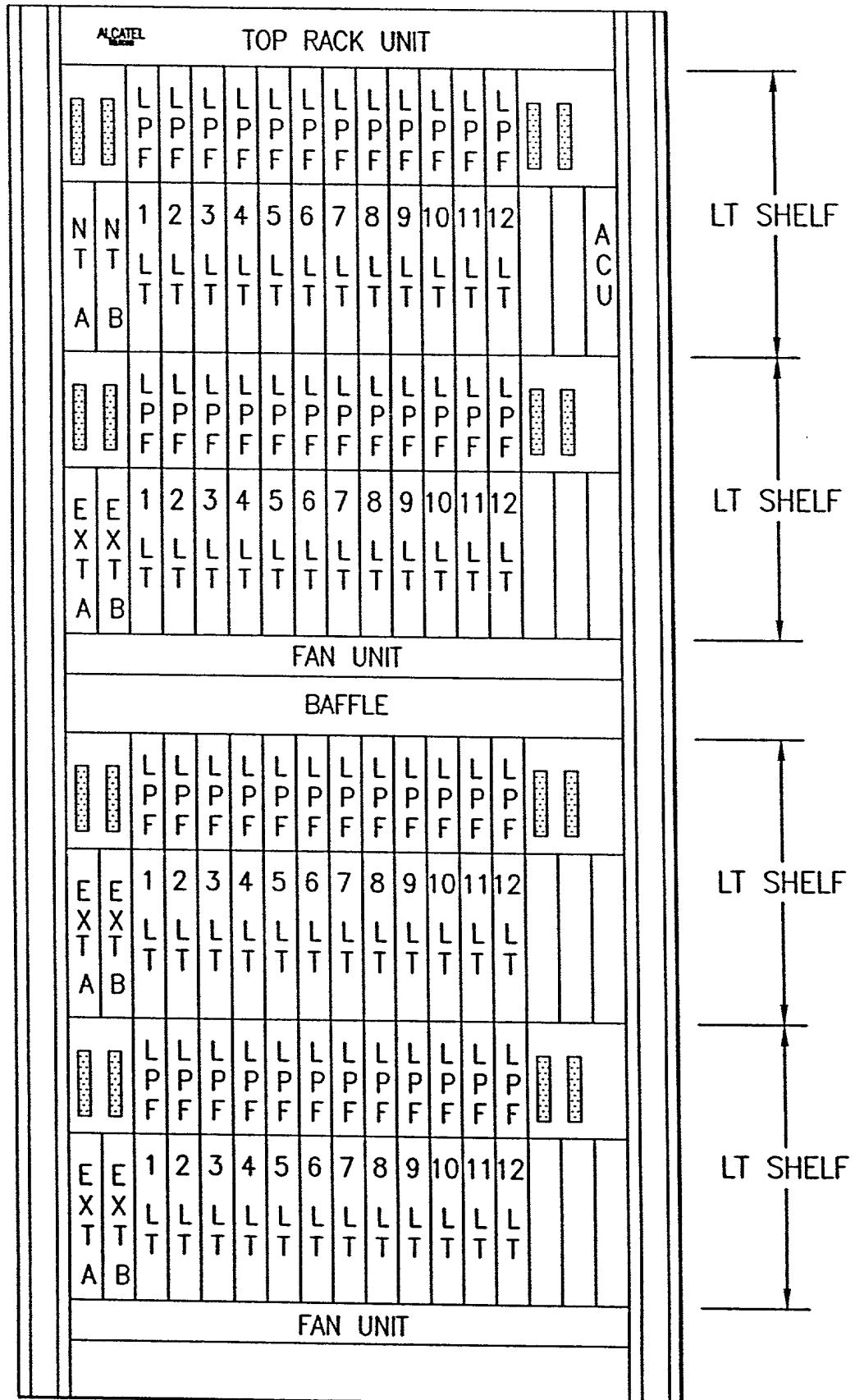


FIG. 1C

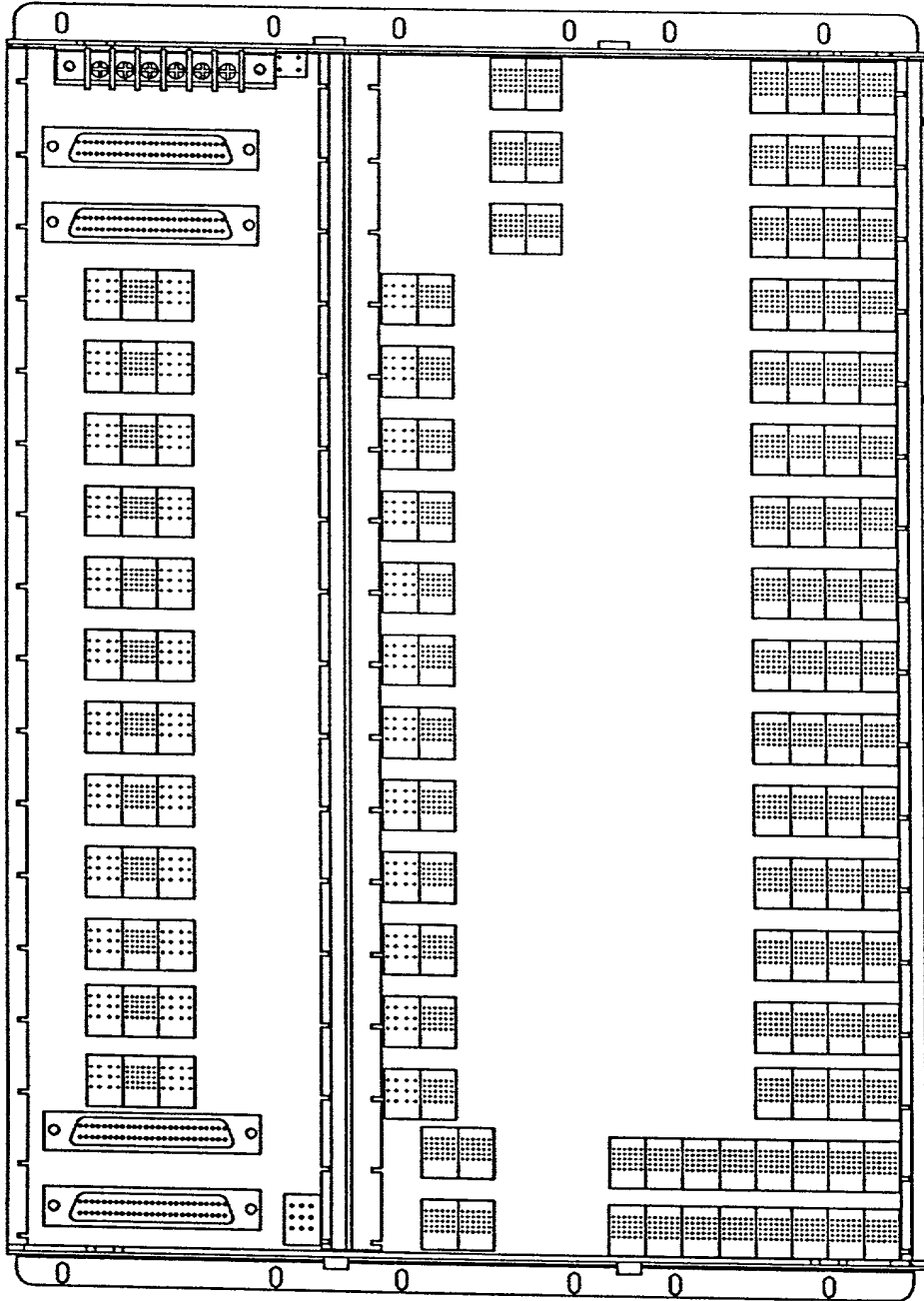


FIG. 1D

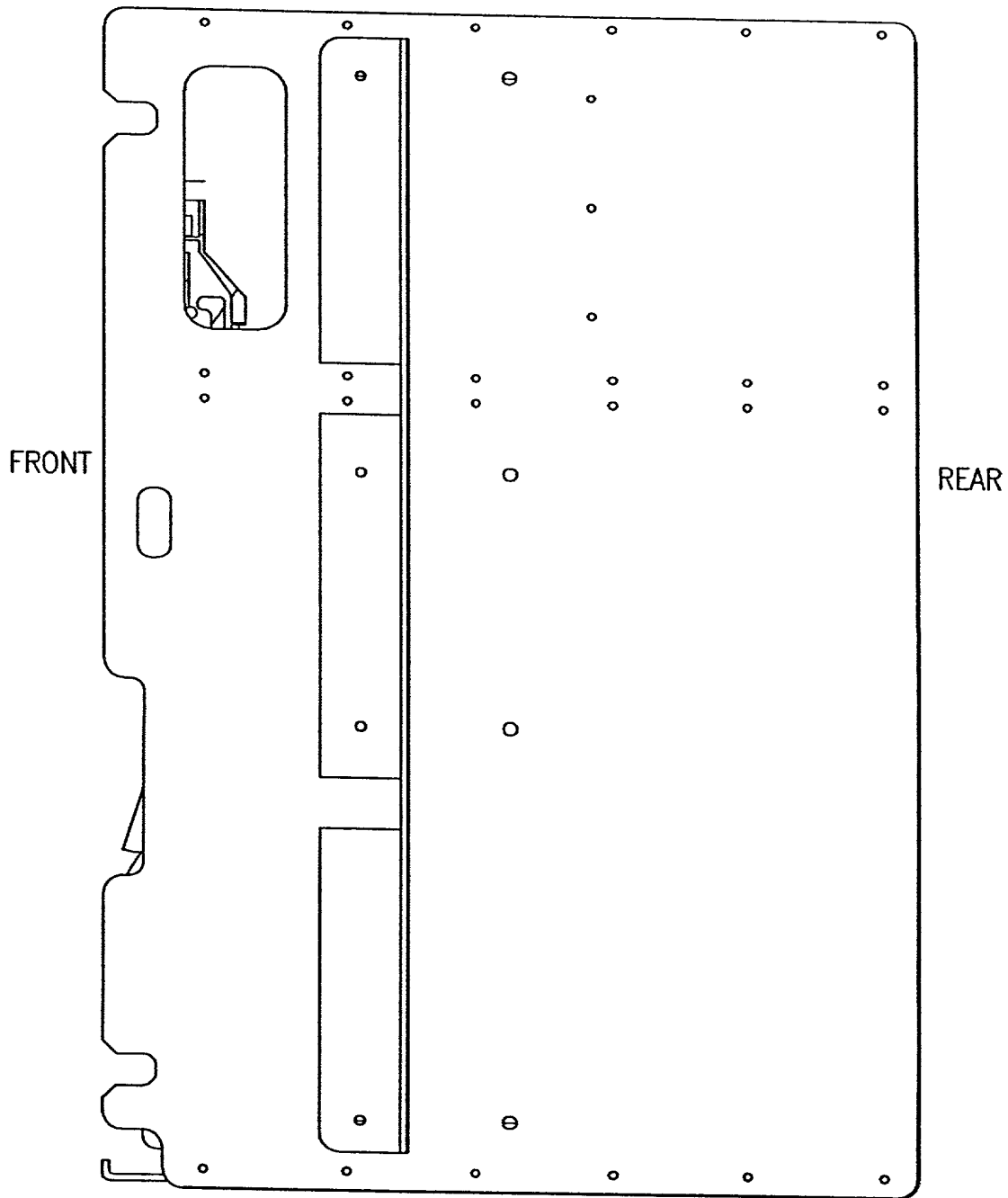


FIG. 1E

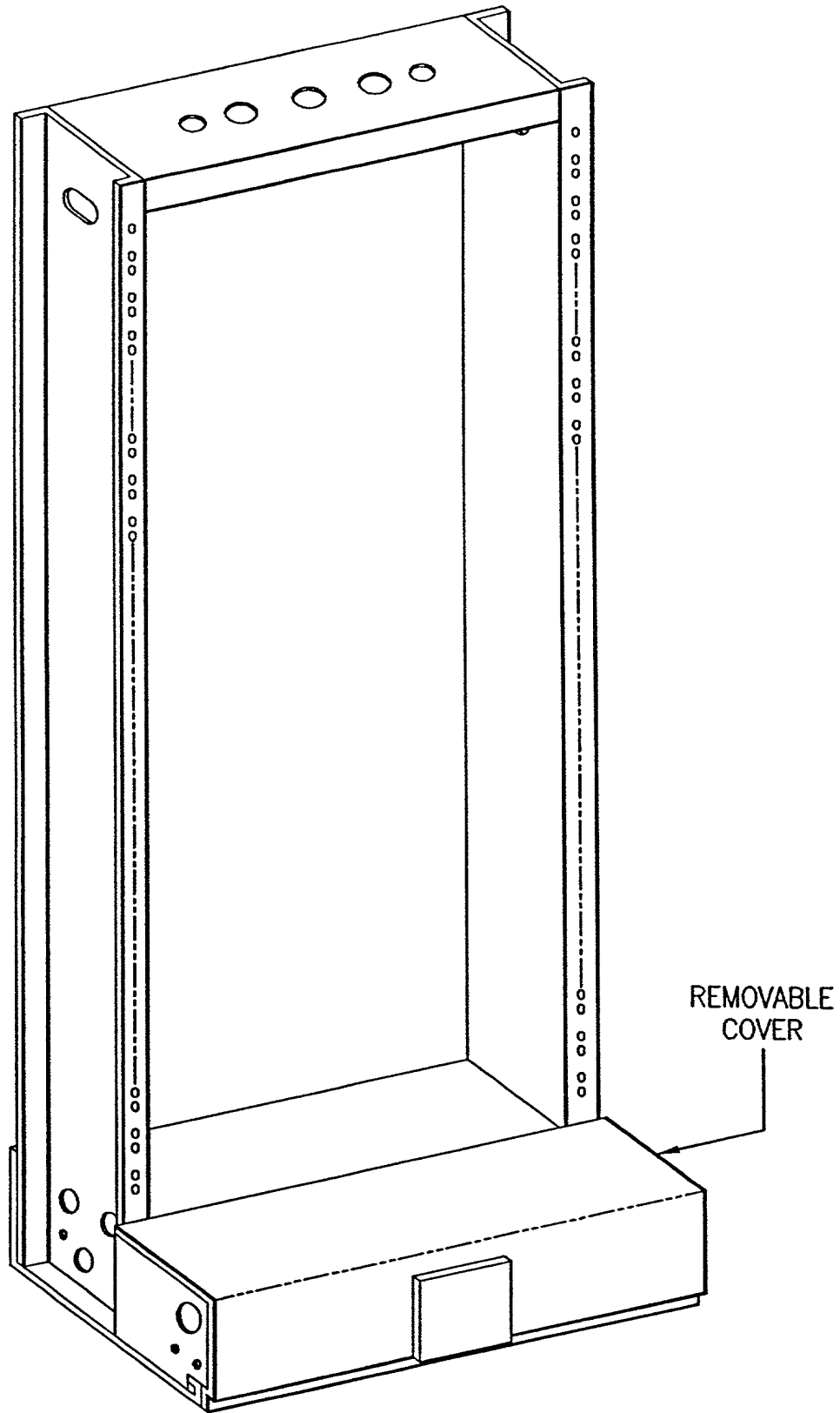


FIG. 3

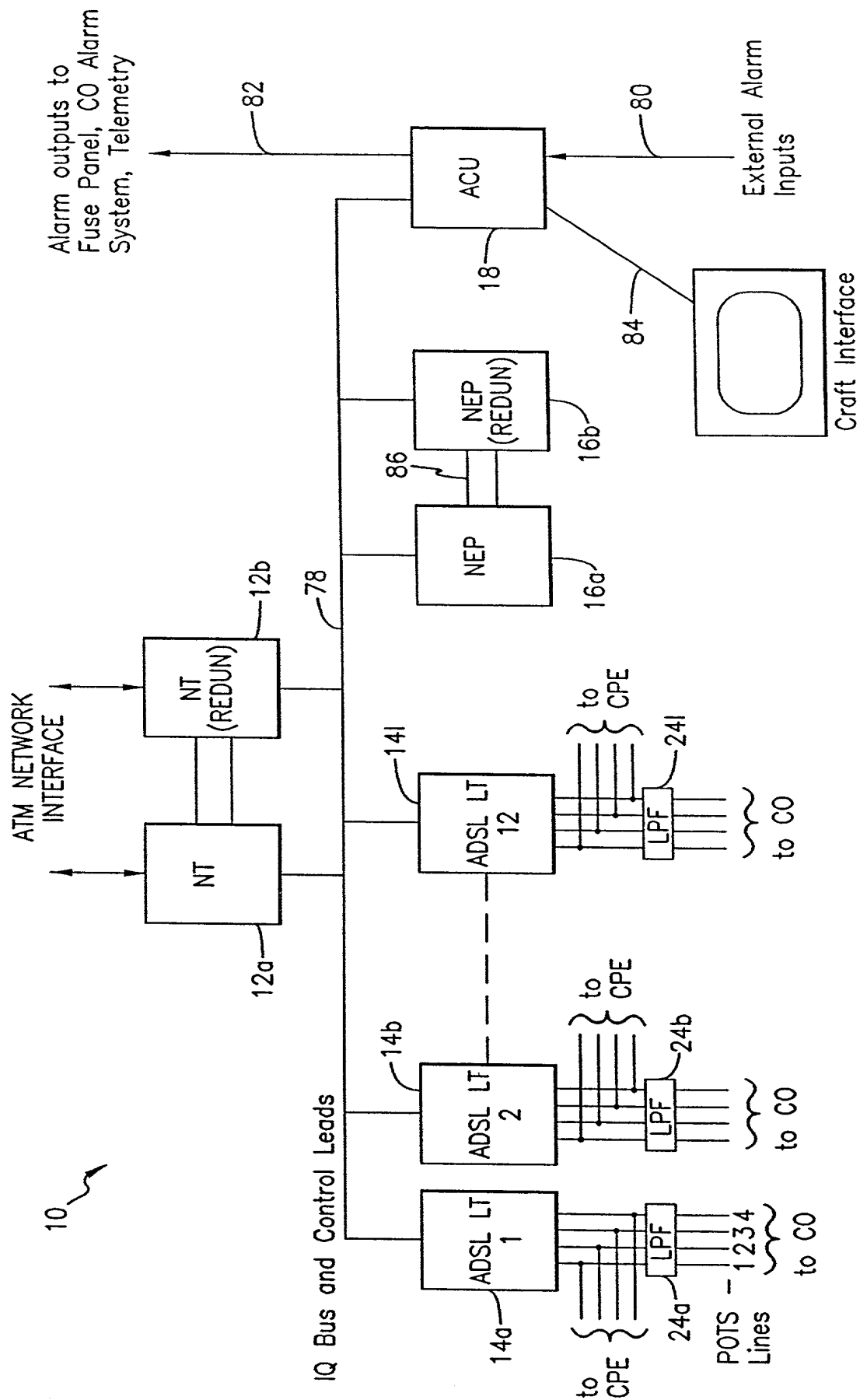


FIG. 3A

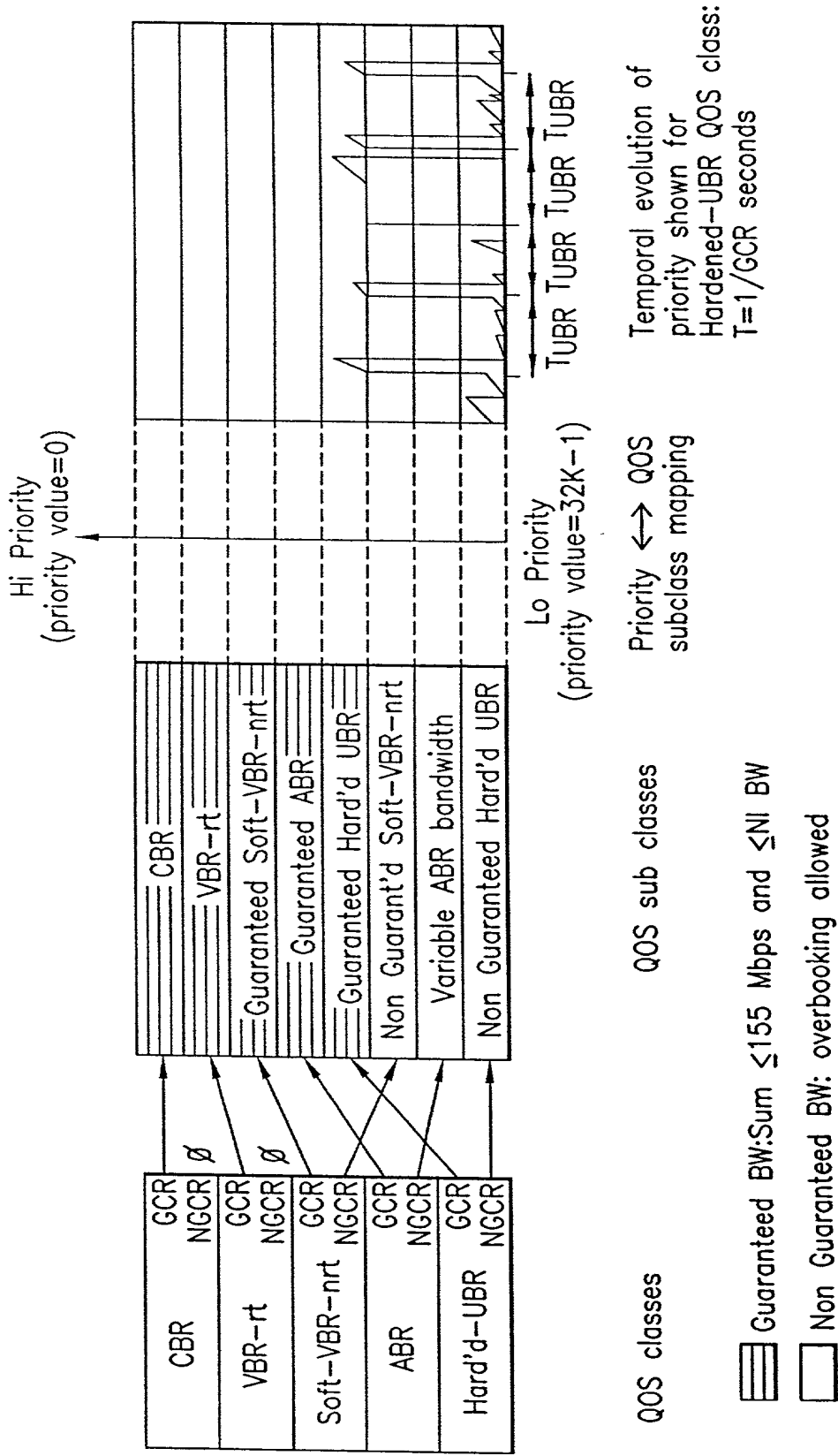


FIG. 4

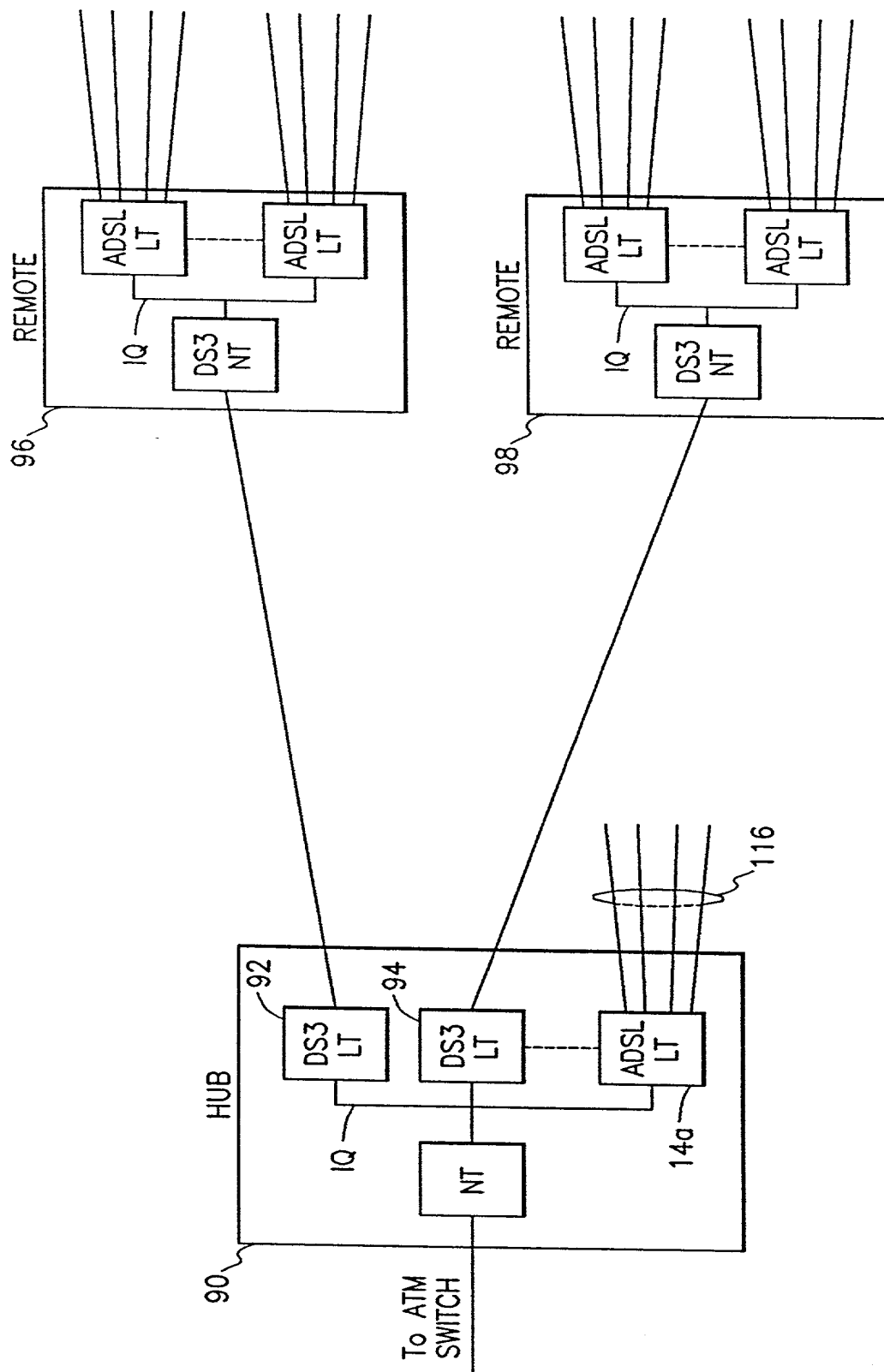


FIG. 4A

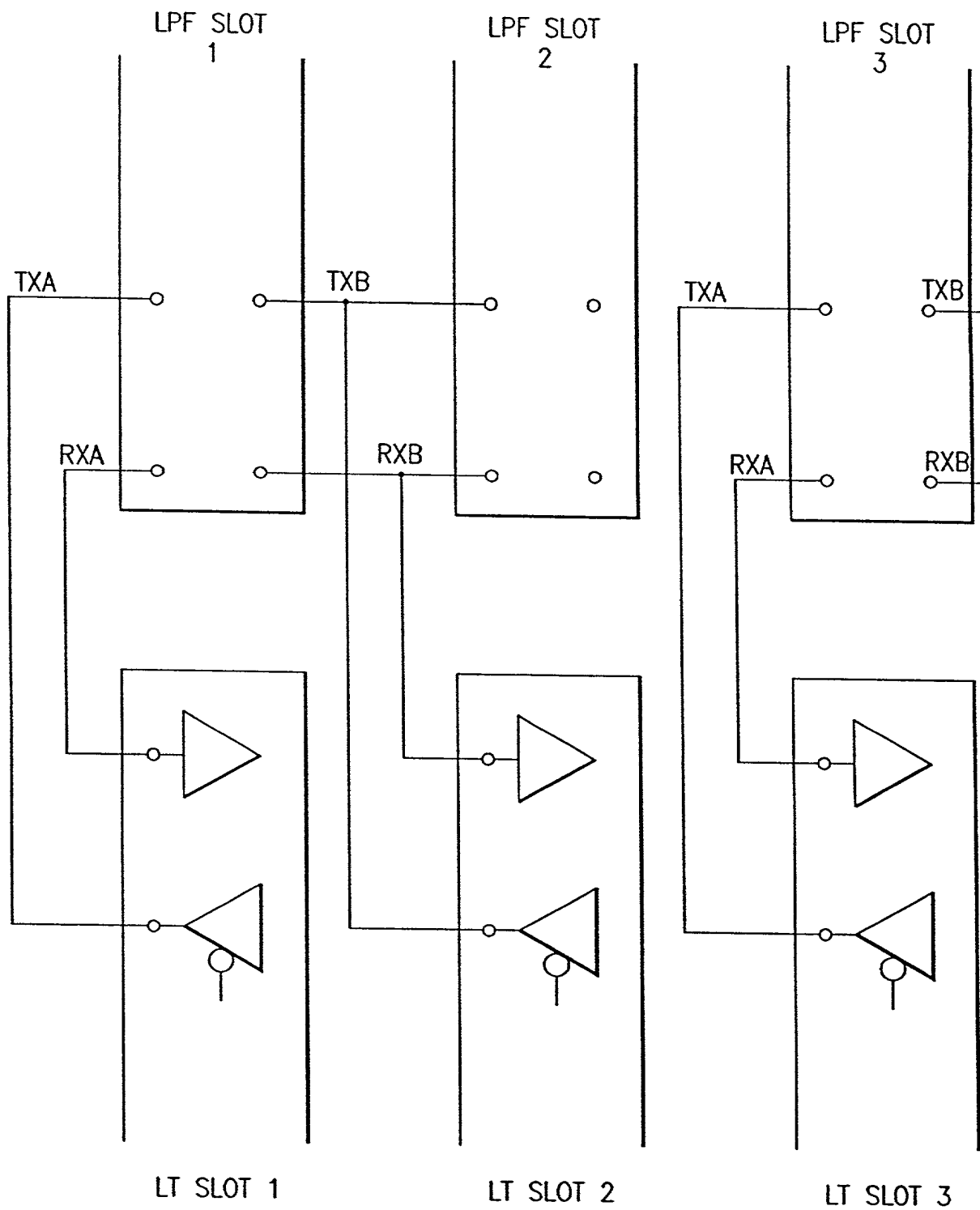
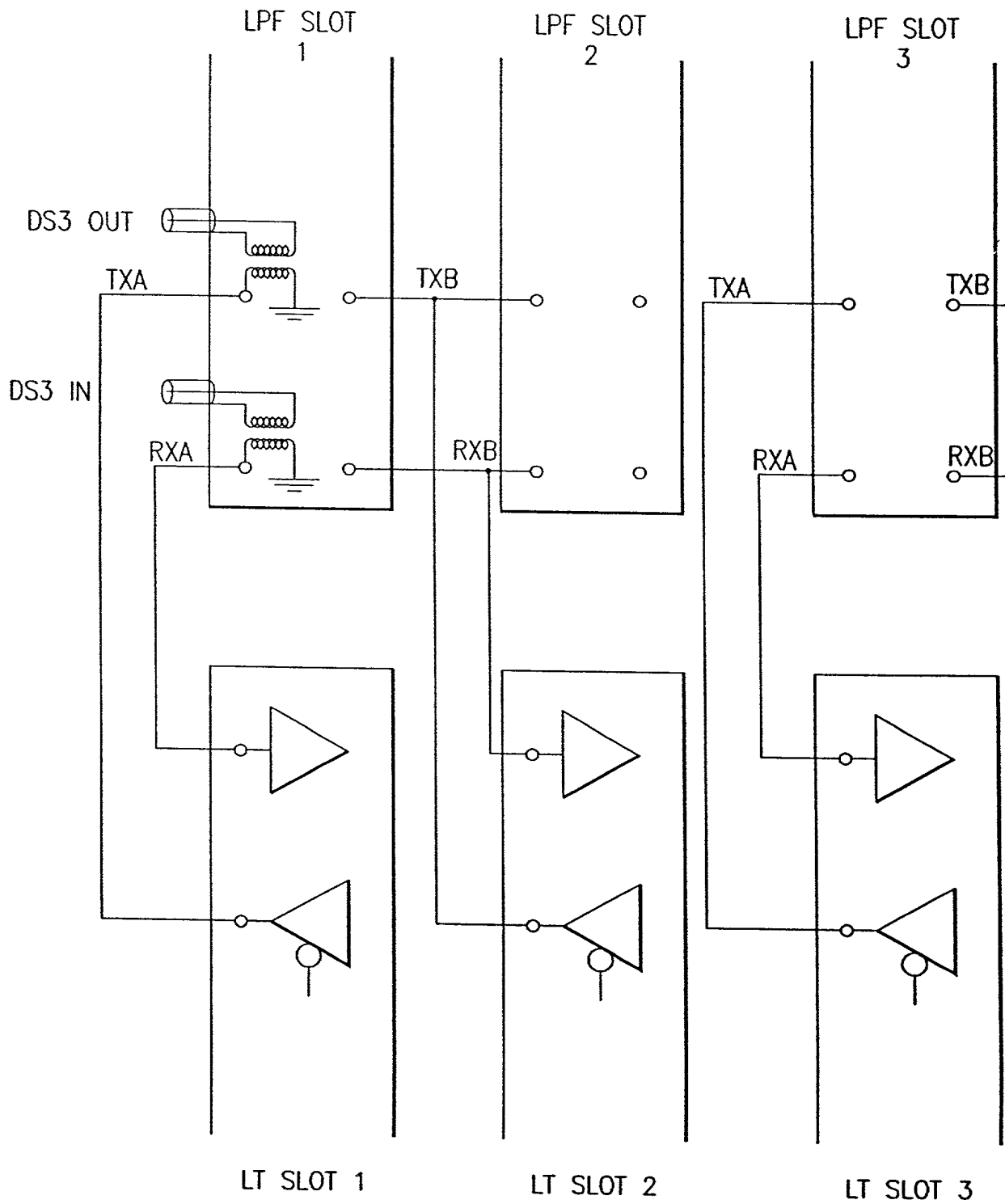


FIG. 4B



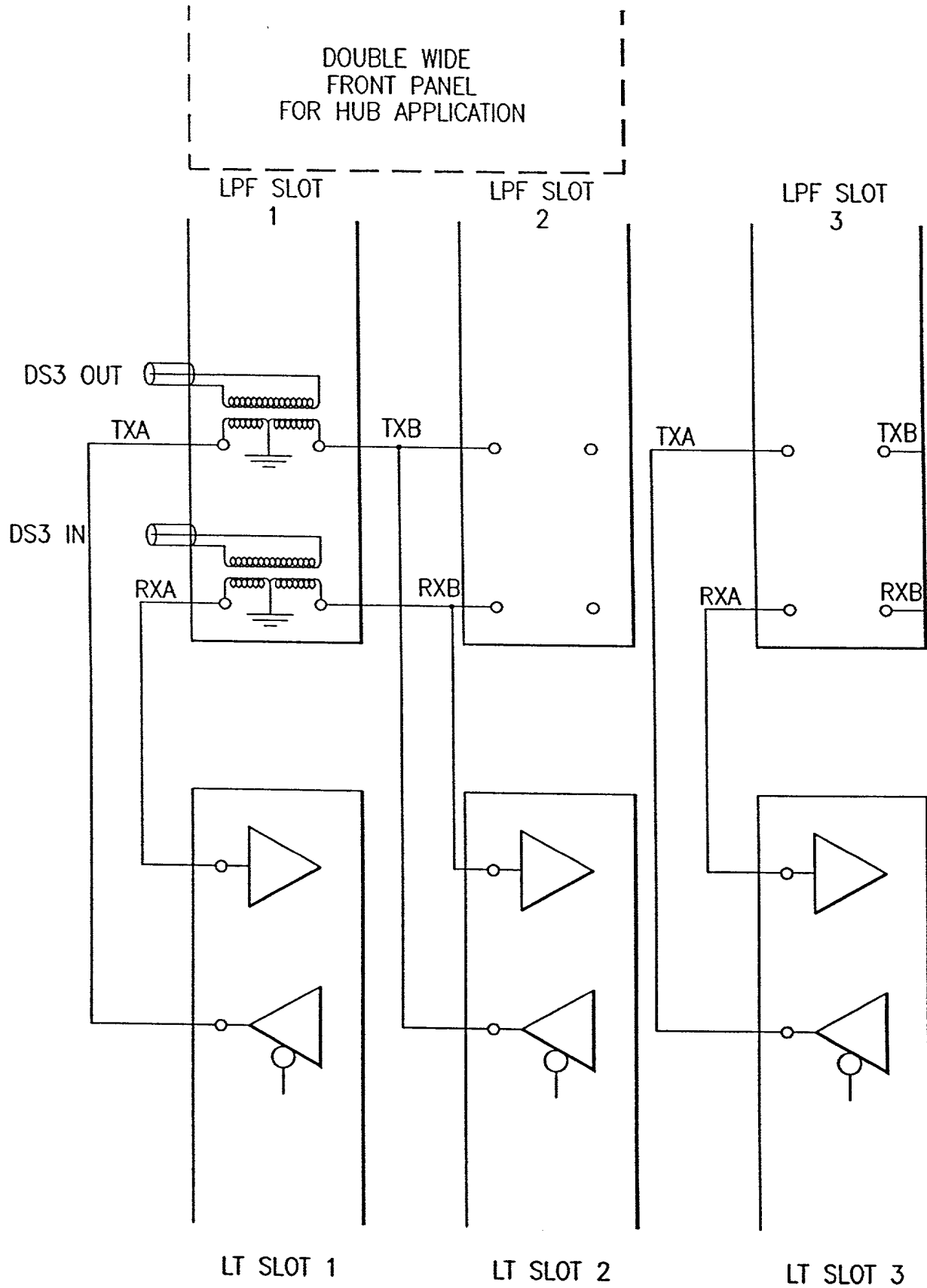
[illegible]

FIG. 4D

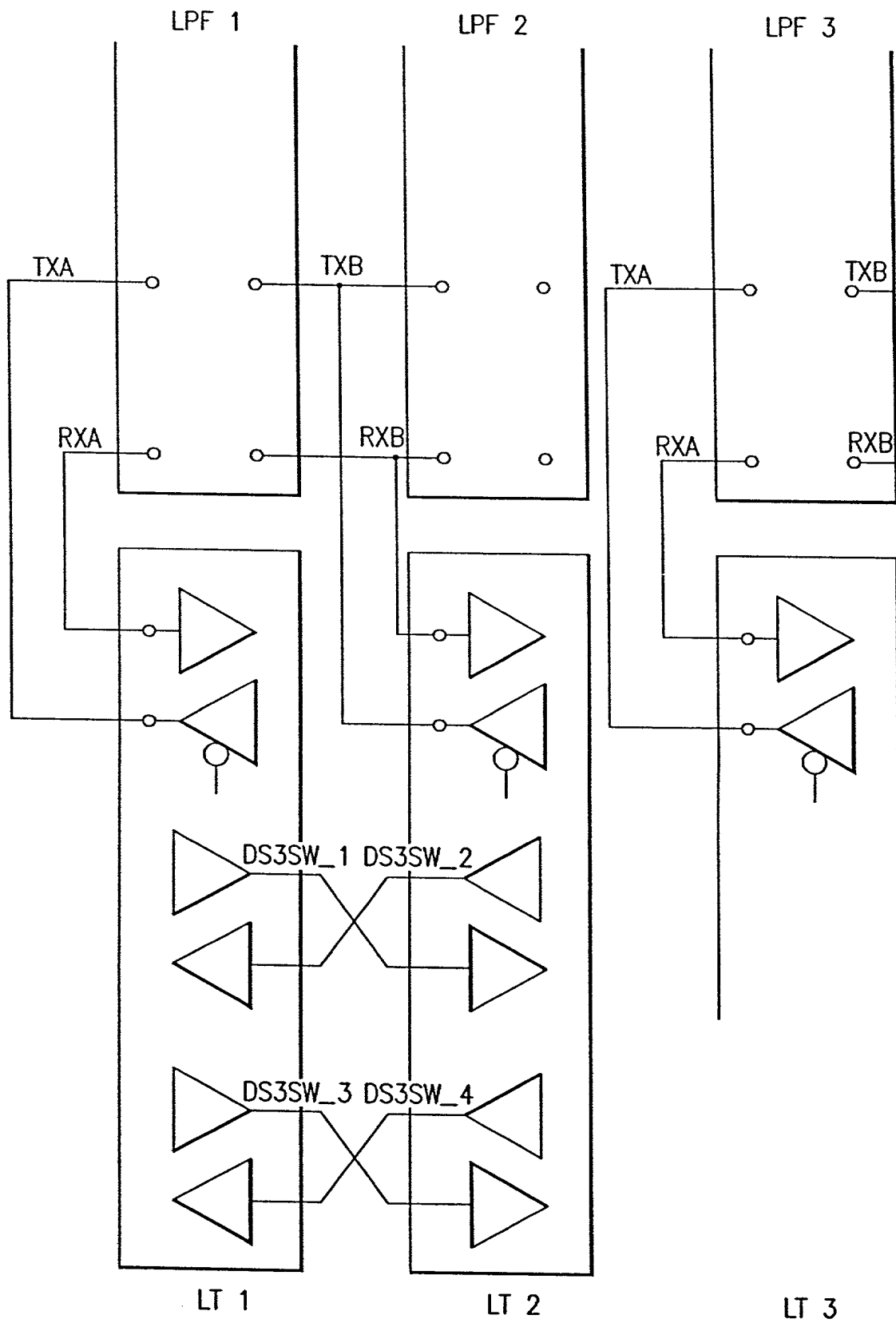
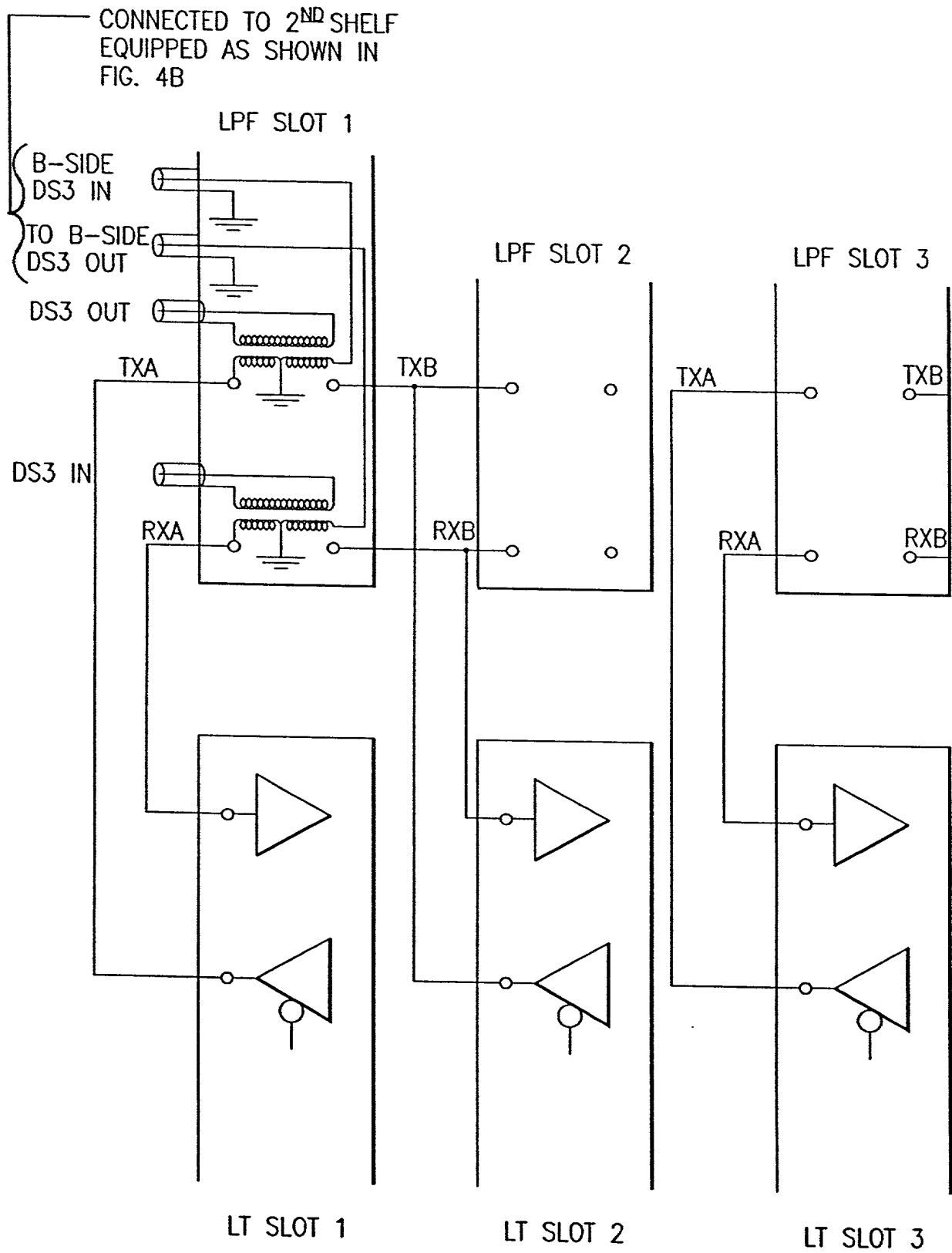


FIG. 4E



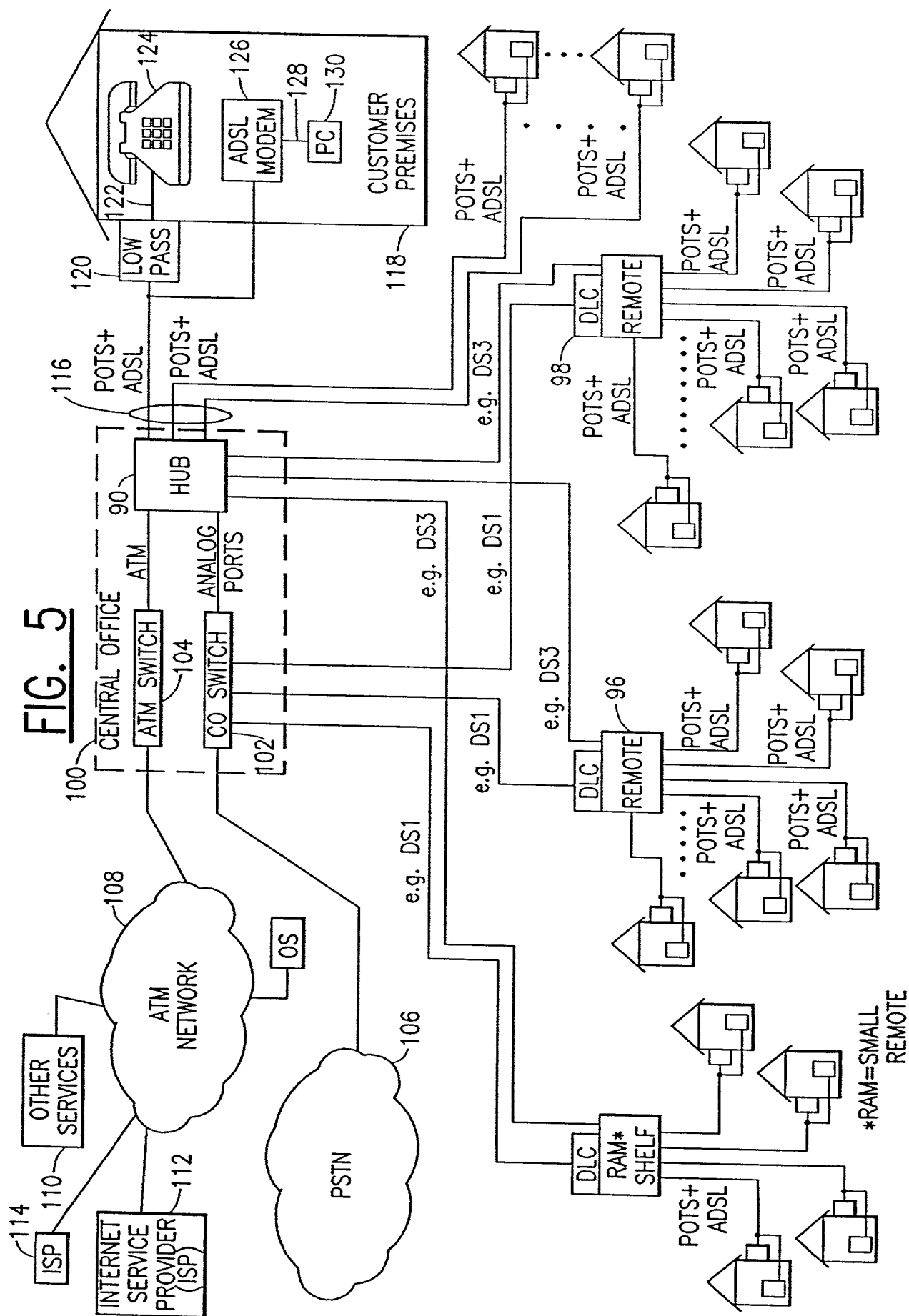


FIG. 6

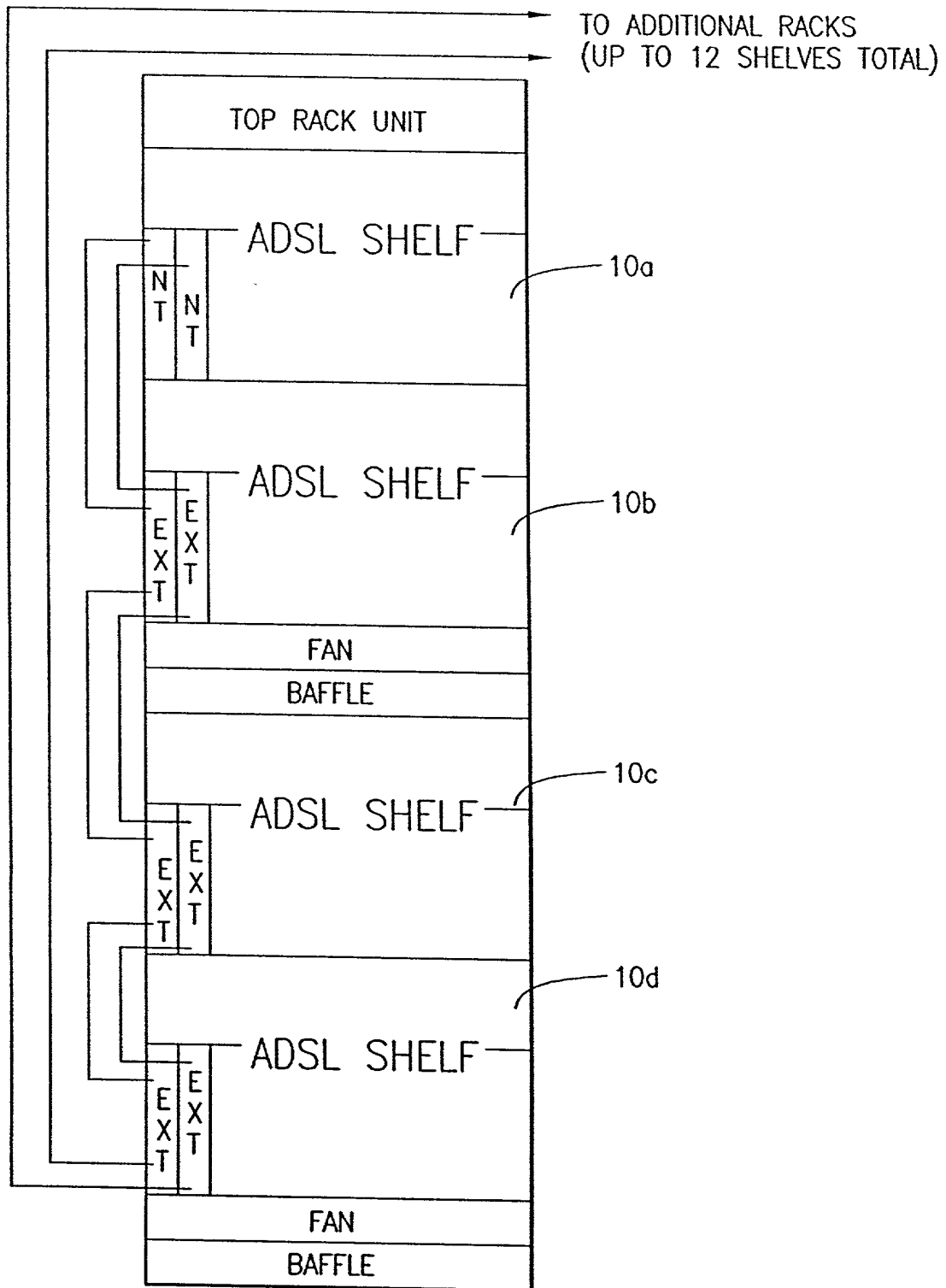


FIG. 7D

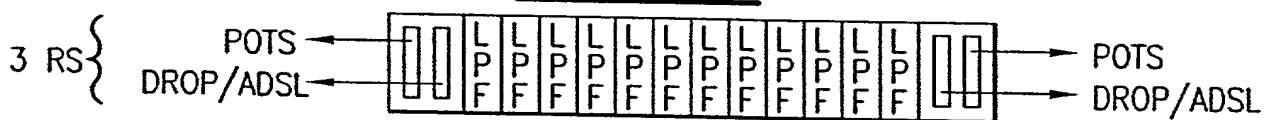


FIG. 7A

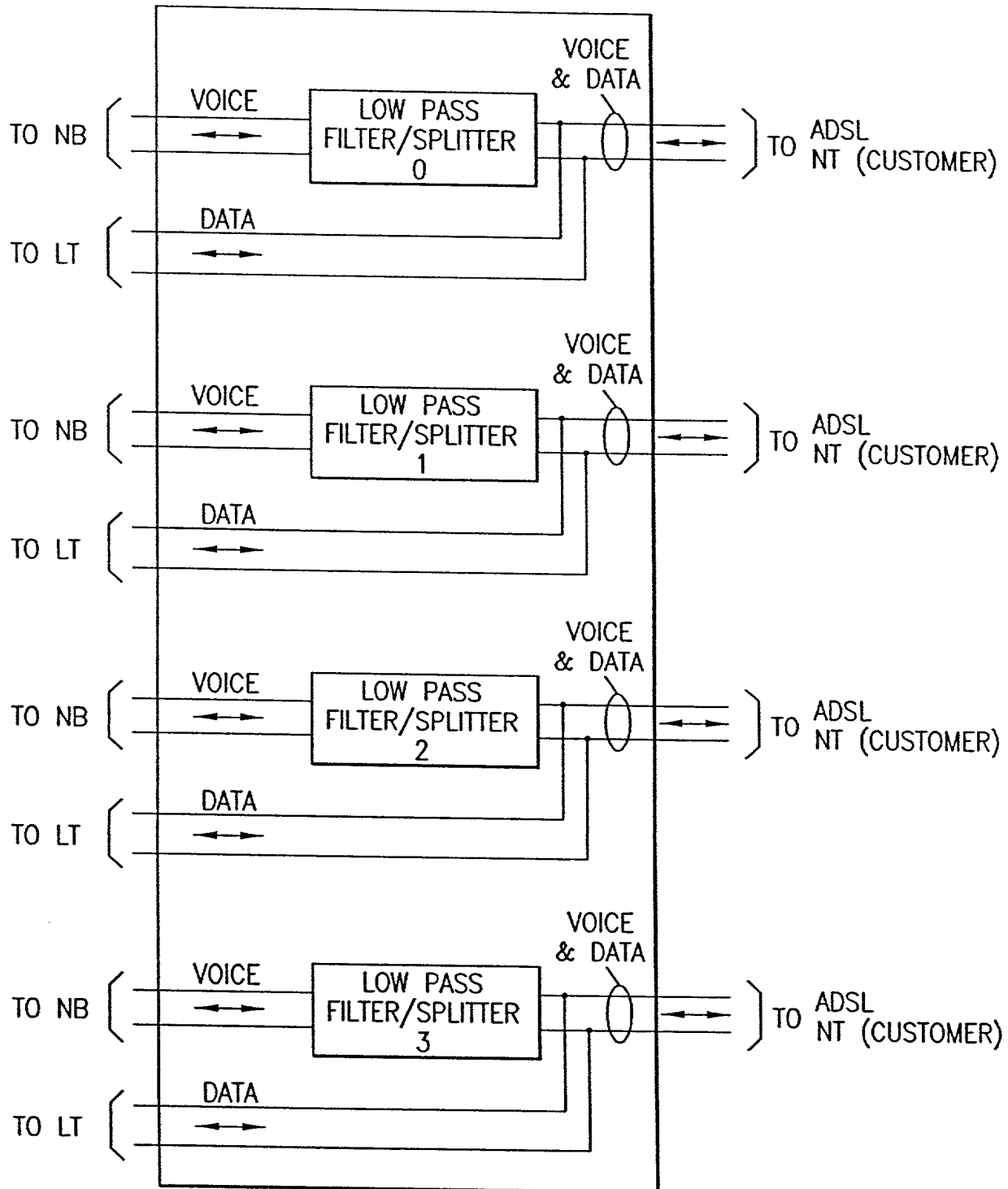


FIG. 7B

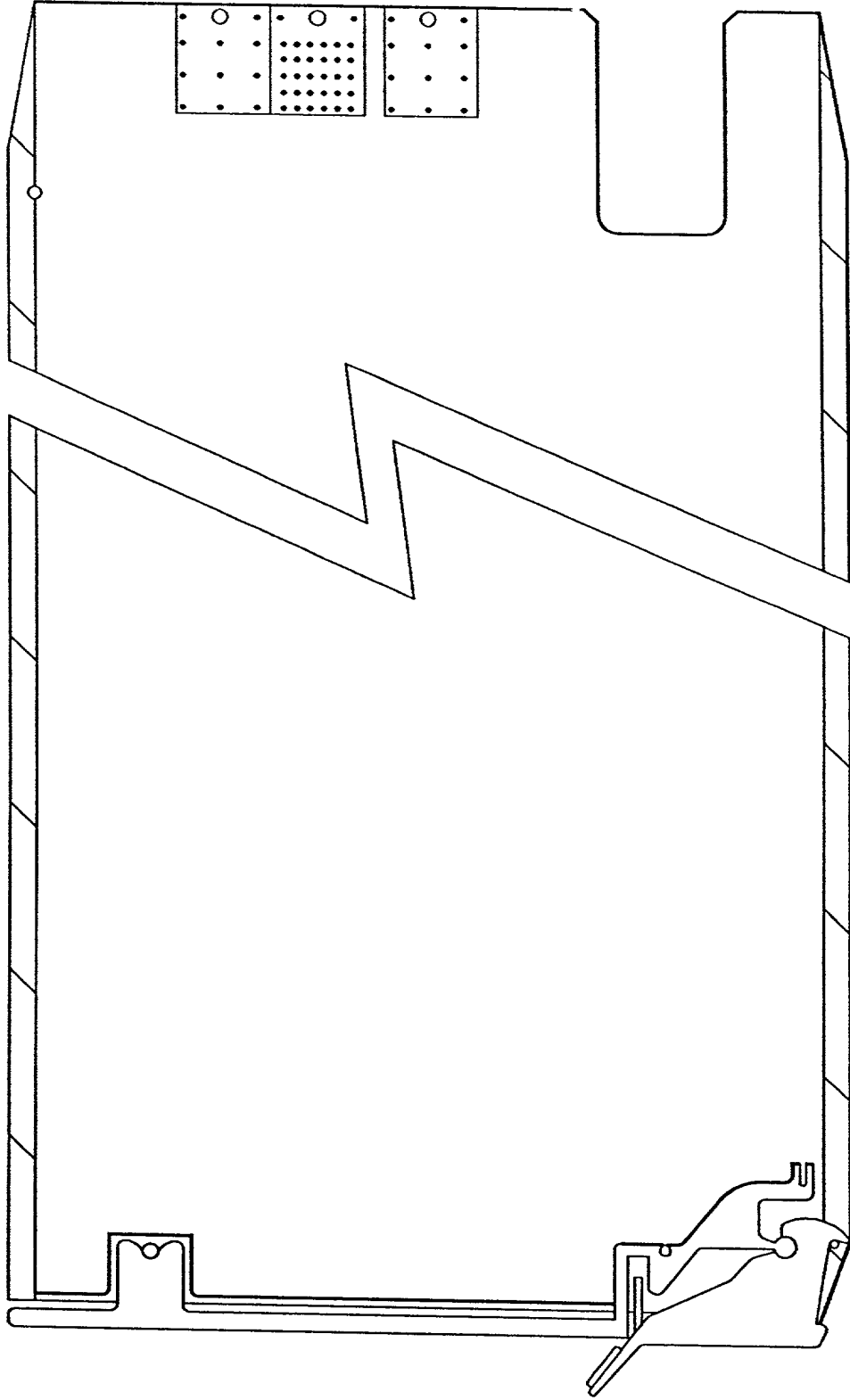


FIG. 7C

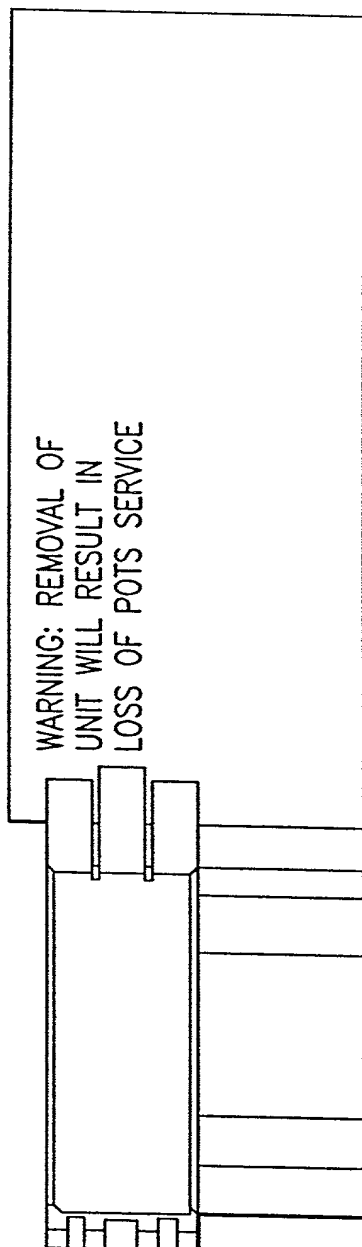


FIG. 8

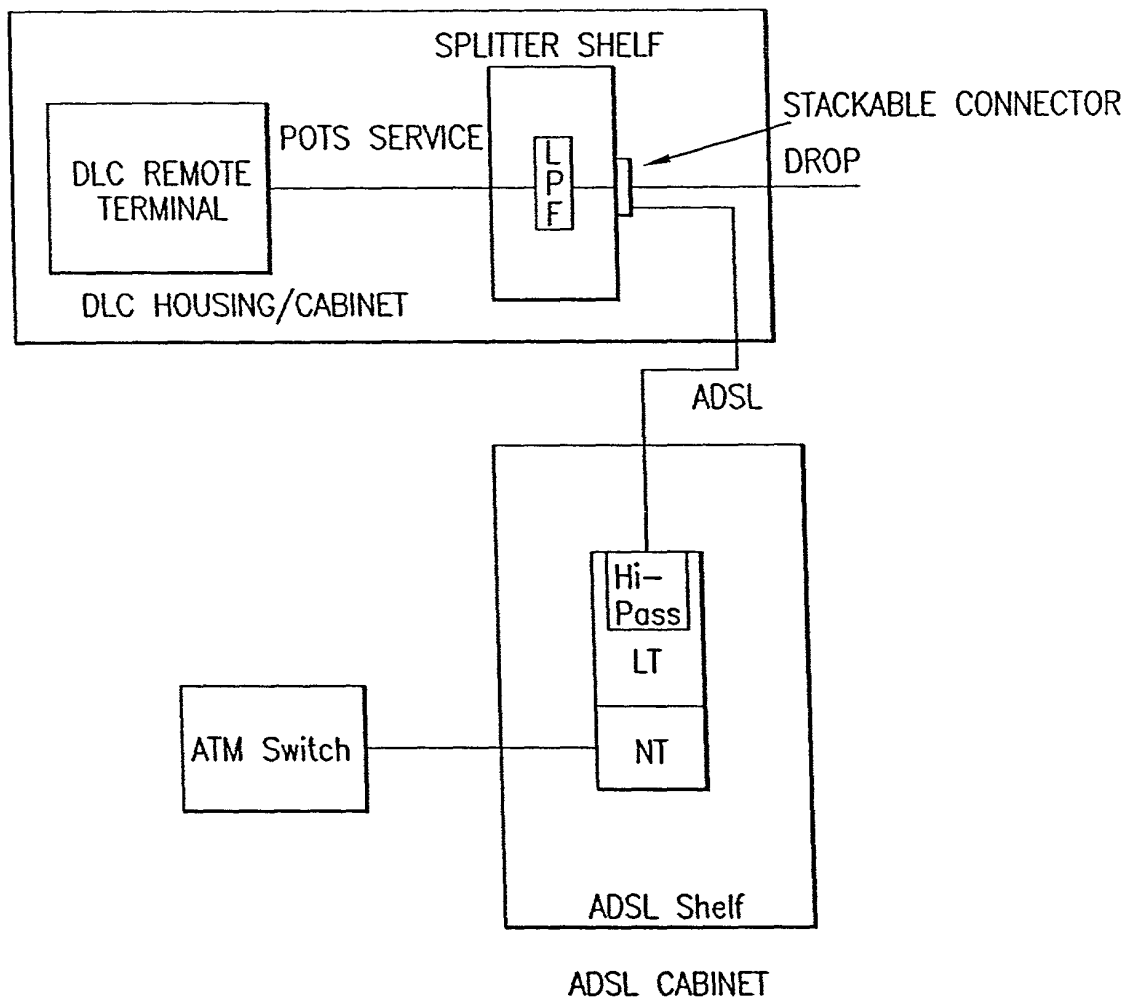


FIG. 13D

| INDICATOR | | MEANING |
|-------------|-------|---------------------------------------|
| NAME | COLOR | |
| ATMF-25 | Green | ATMF data transport activity |
| TX/RX | Green | Data transmit/receive |
| Line Error | Red | Excessive line errors-bad ADSL line |
| 10 Base-T | Green | Ethernet data transport activity |
| Power/Sync. | Red | Power-on - initialization phase |
| | Green | Line synchronization-ready to operate |

FIG. 8A

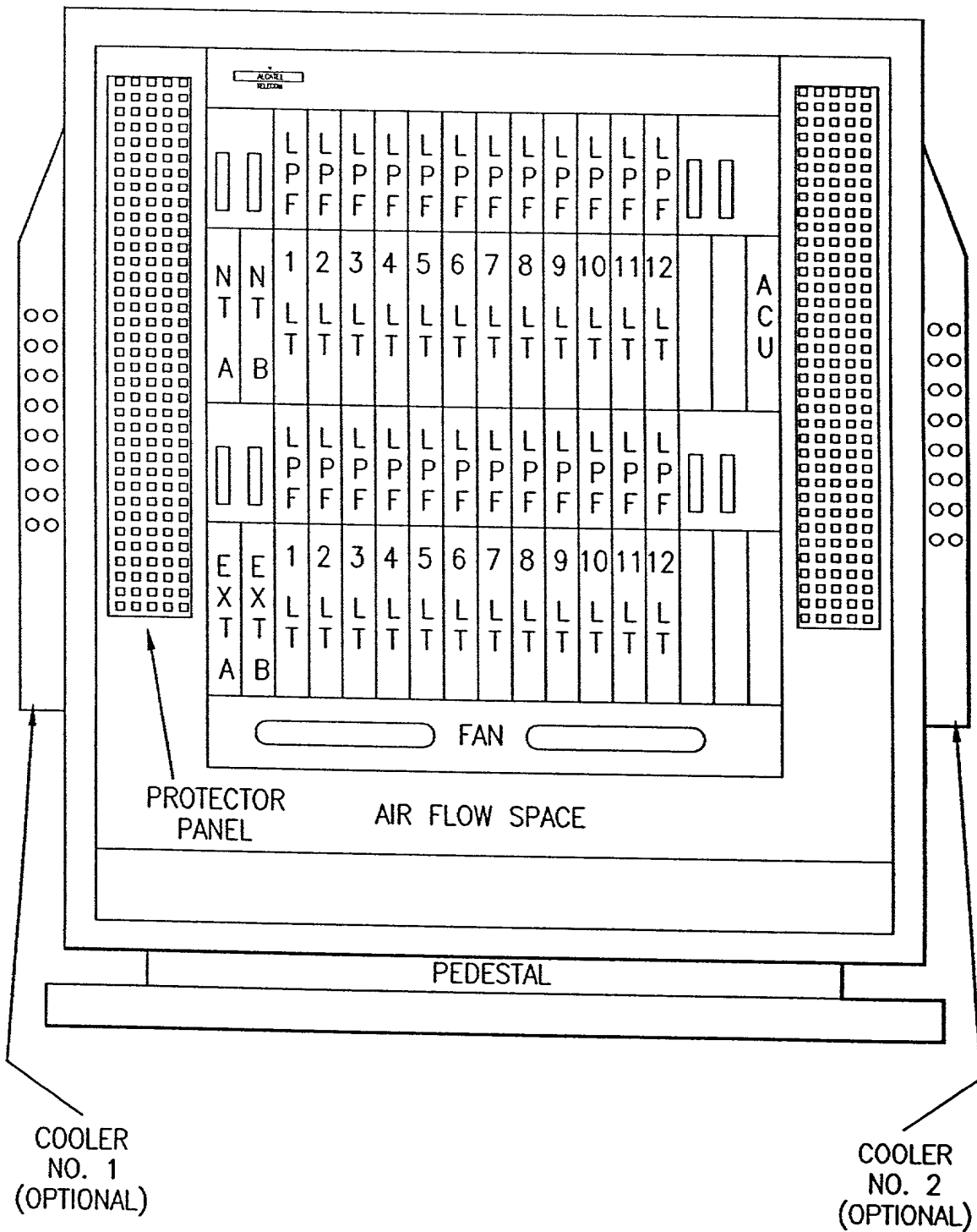
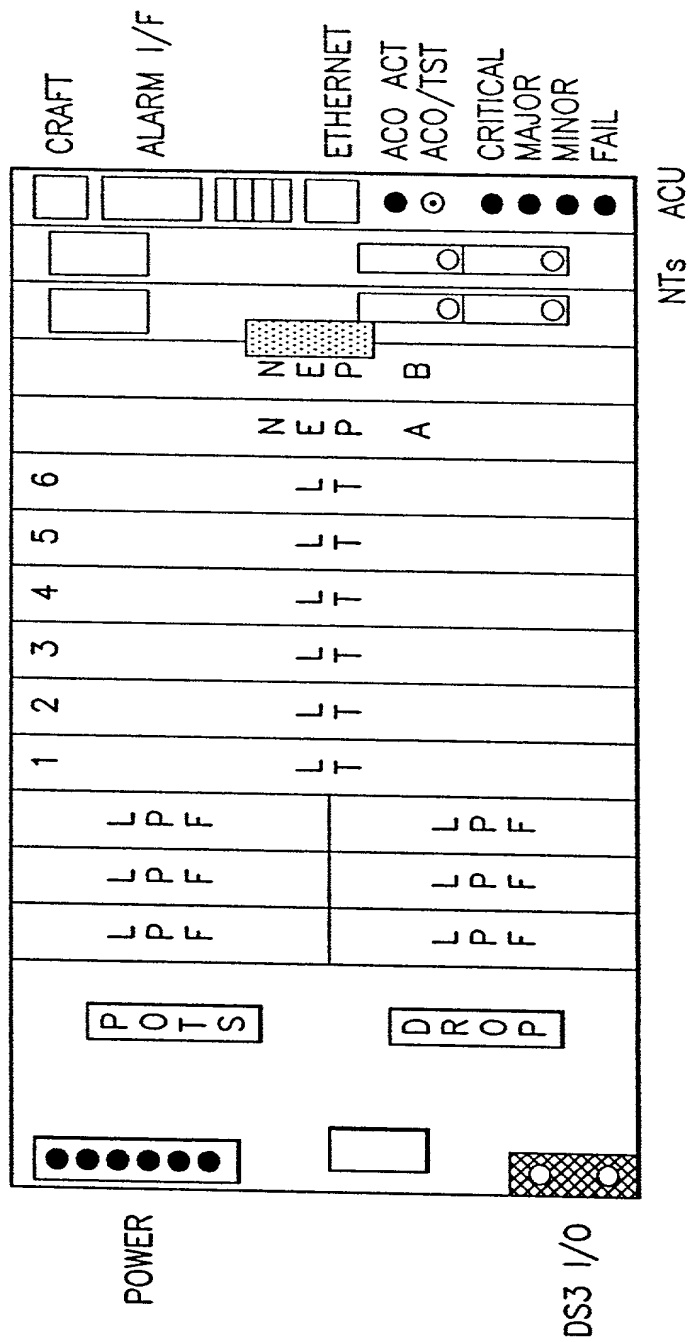


FIG. 9



14a

FIG. 10

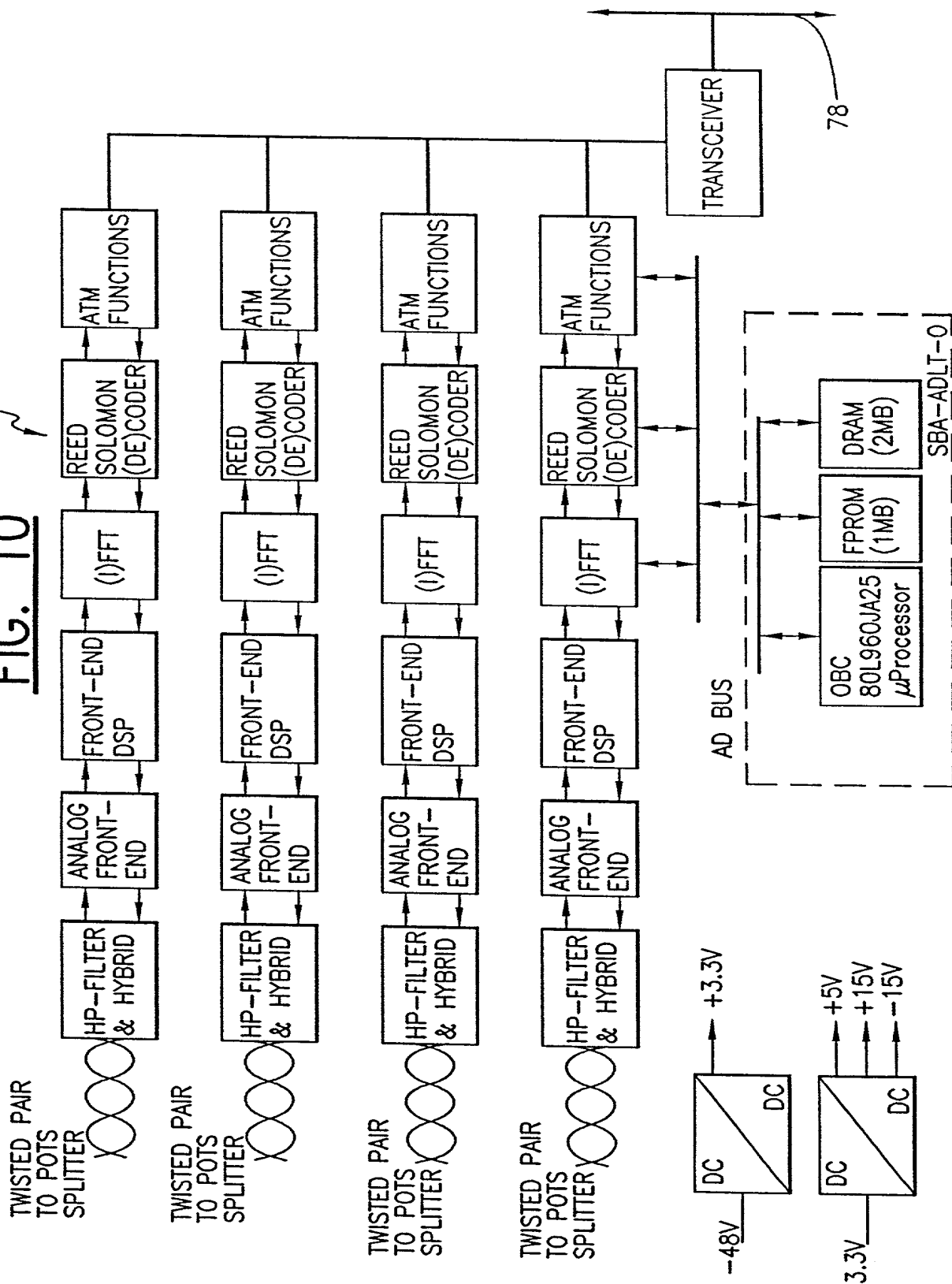


FIG. 10A

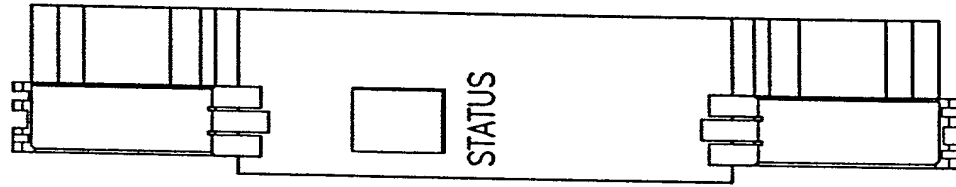


FIG. 10B

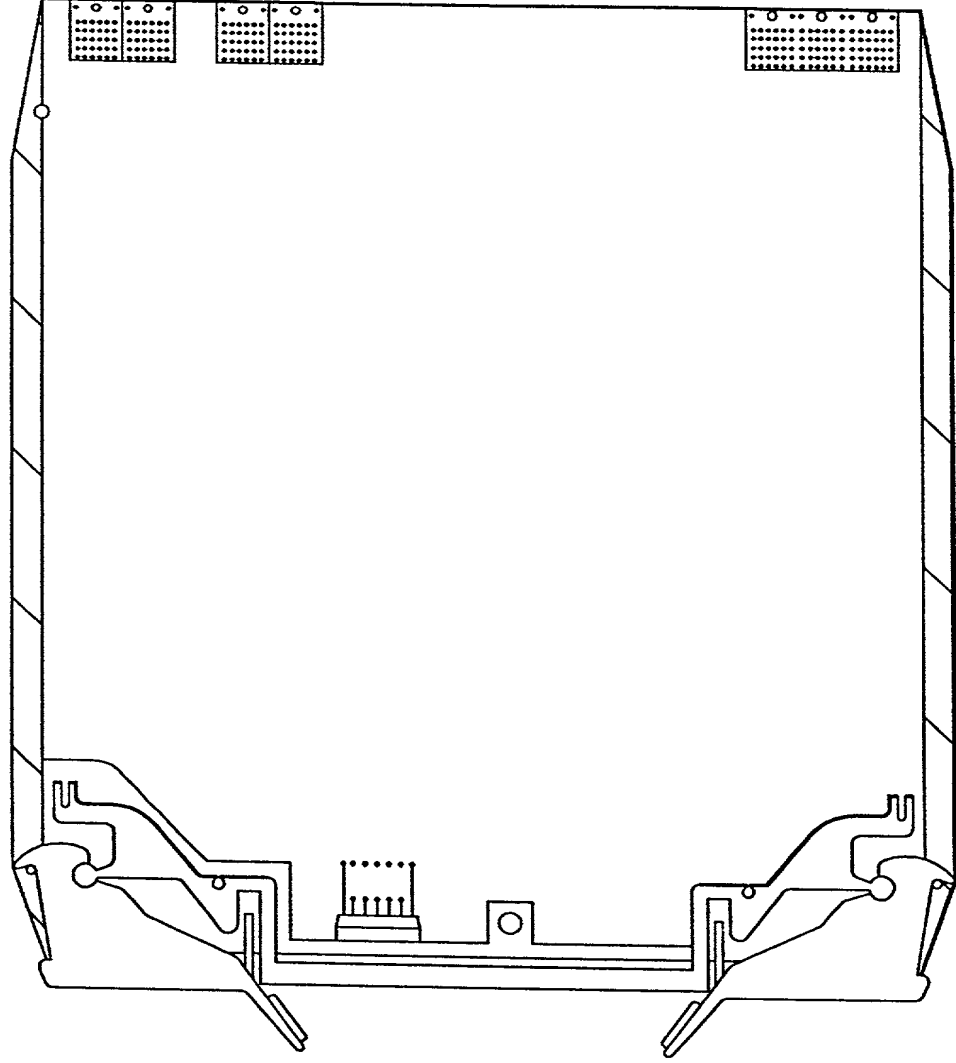


FIG. 11

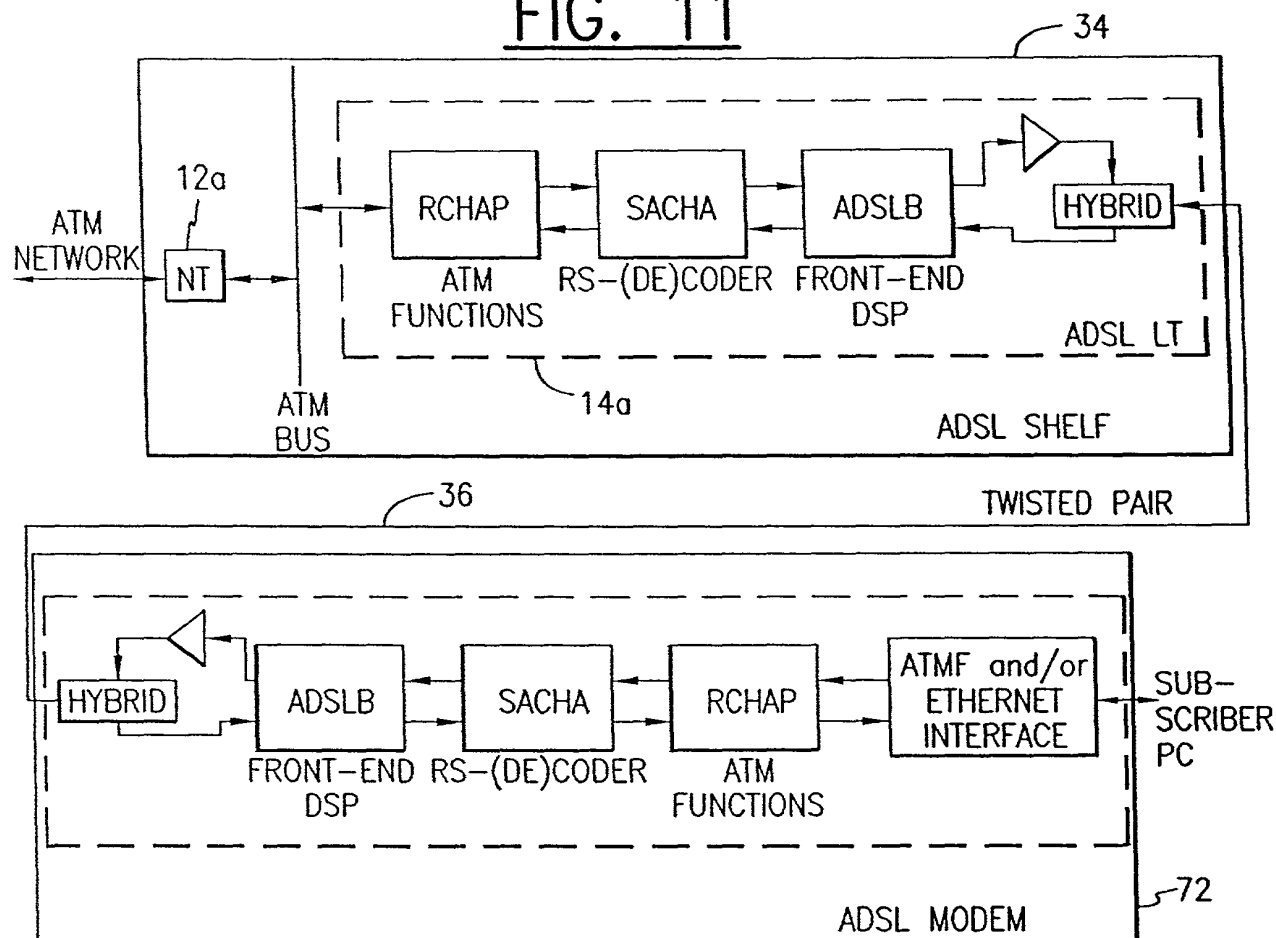


FIG. 12

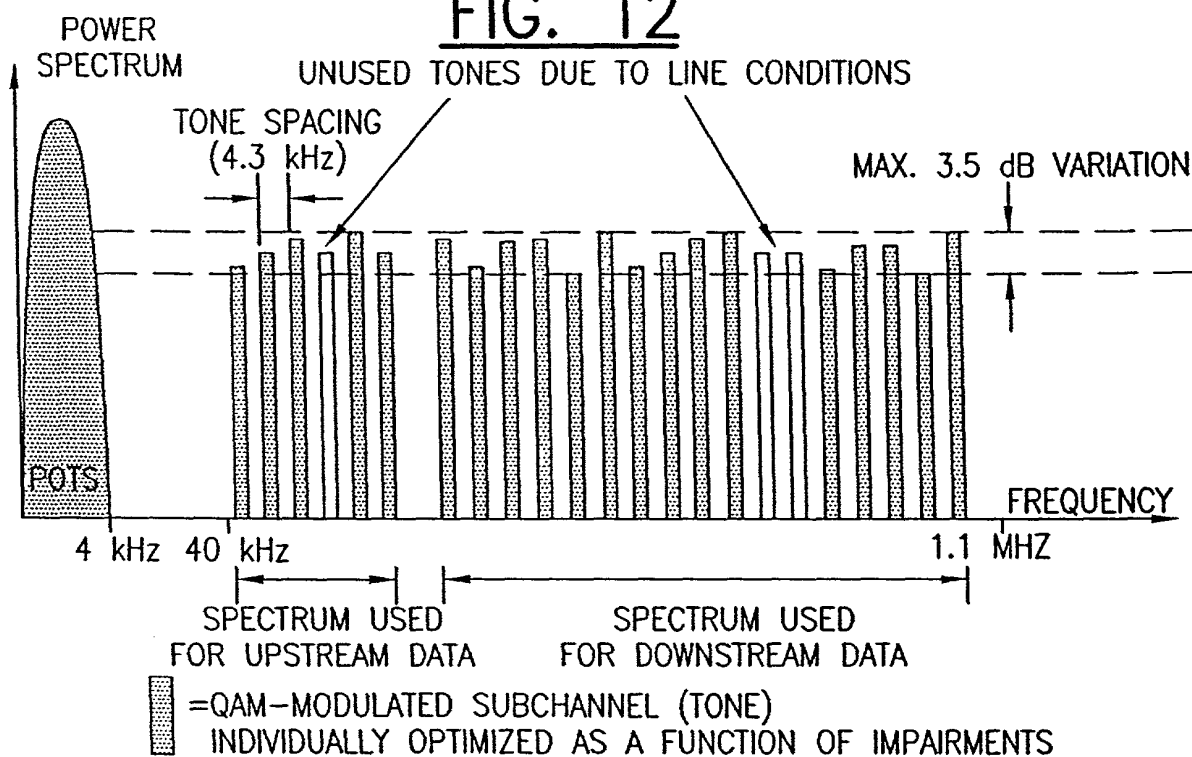


FIG. 13A

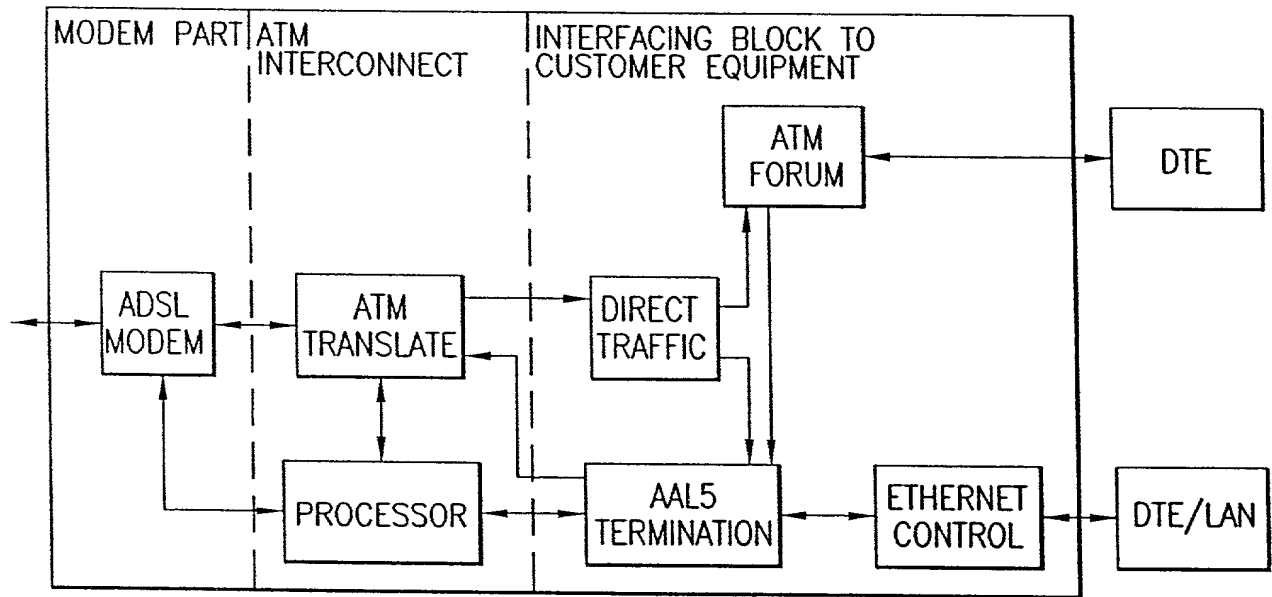


FIG. 13B

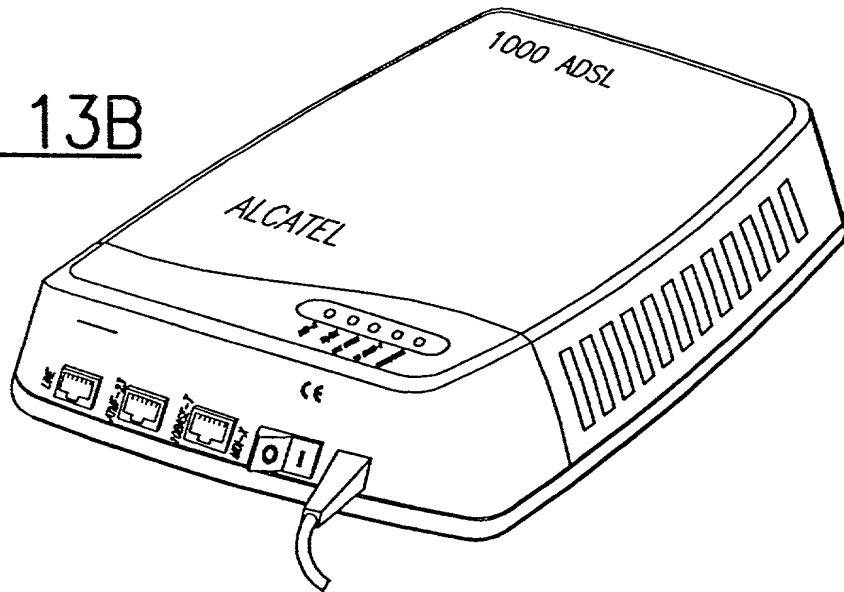


FIG. 13C

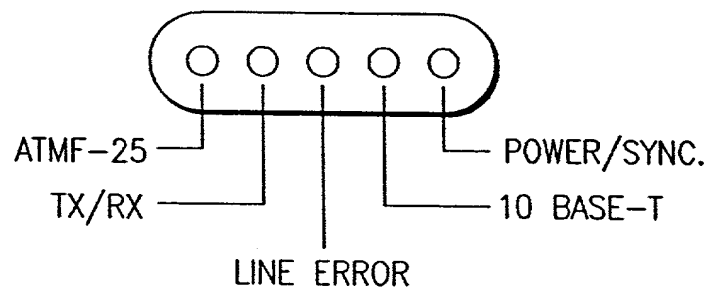


FIG. 13E

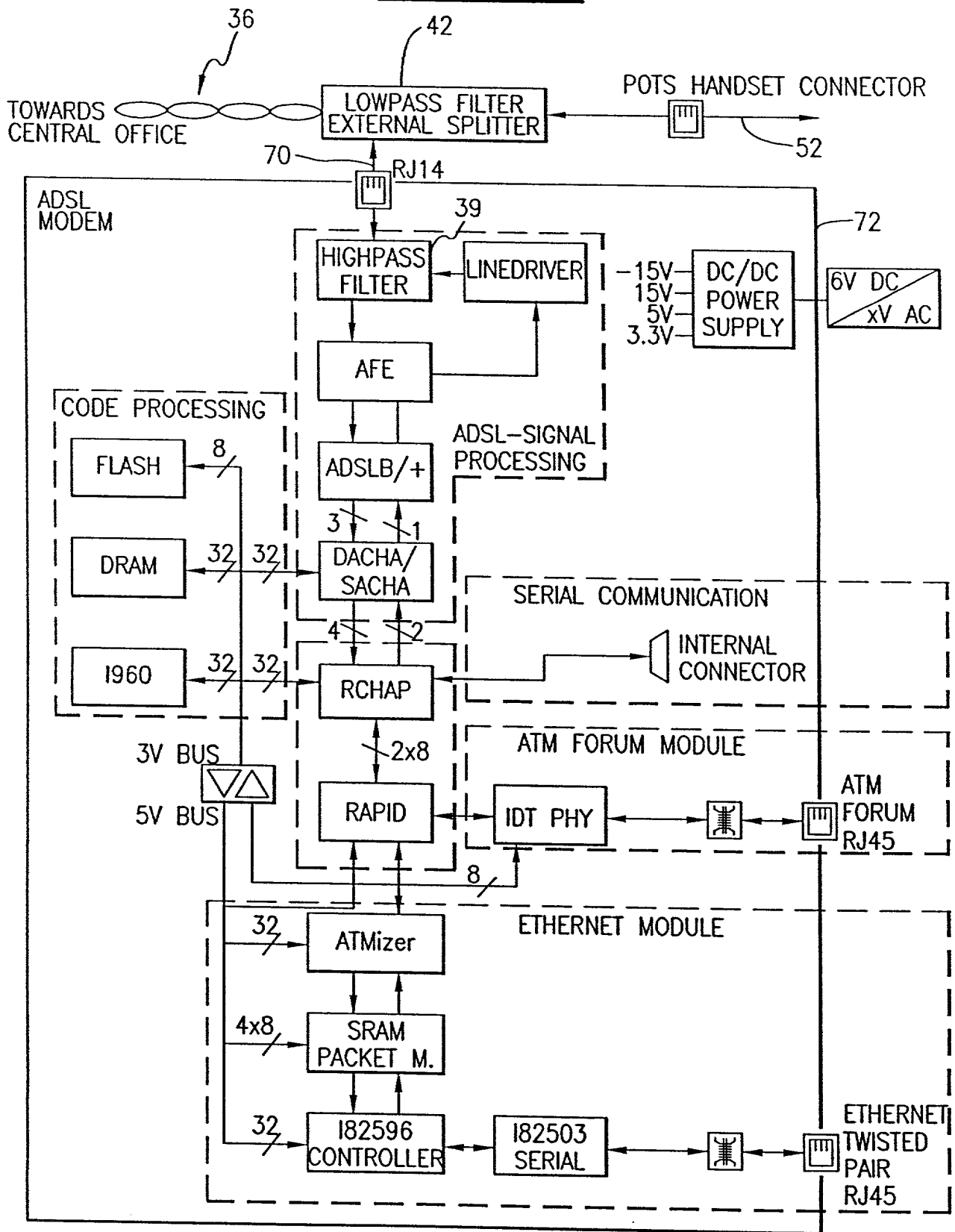


FIG. 14B

| DOWNSTREAM† FUNCTIONS | | UPSTREAM† FUNCTIONS | |
|-----------------------|---|--|---|
| ① | Optical interface | Reading ATM cells from the ATM interface (IQ BUS) | ⑤ |
| | Locking on received clock | ATM cell extraction | |
| | Serial to parallel conversion | ATM cell insertion | |
| ② | STM1/STS3c frame alignment recovery | ATM layer processing plus cell rate decoupling | ⑥ |
| | STM1/STS3c descrambling | ATM cell Header Error Control (HEC) calculation | |
| | F1, F2, or F3 OAM functions | ATM cell payload scrambling | |
| ③ | ATM cell delineation (in virtual container type 4s) | Mapping of ATM cells in virtual container type 4s | ⑦ |
| | ATM cell HEC checking | F1, F2, or F3 OAM functions | |
| | ATM cell payload descrambling | STM1/STS3c scrambling | |
| ④ | ATM layer processing plus cell rate decoupling | STM1/STS3c frame generation | ⑧ |
| | ATM cell extraction | Parallel to serial conversion | |
| | ATM cell insertion | Produce transmit clock out of recieved clock or local oscillator | |
| ④ | Provision of access to the ATM IQ bus | Optical interface | |

Note †Upstream is in the direction of the transport system and downstream is in the direction of the ATM IQ interface.

FIG. 14A

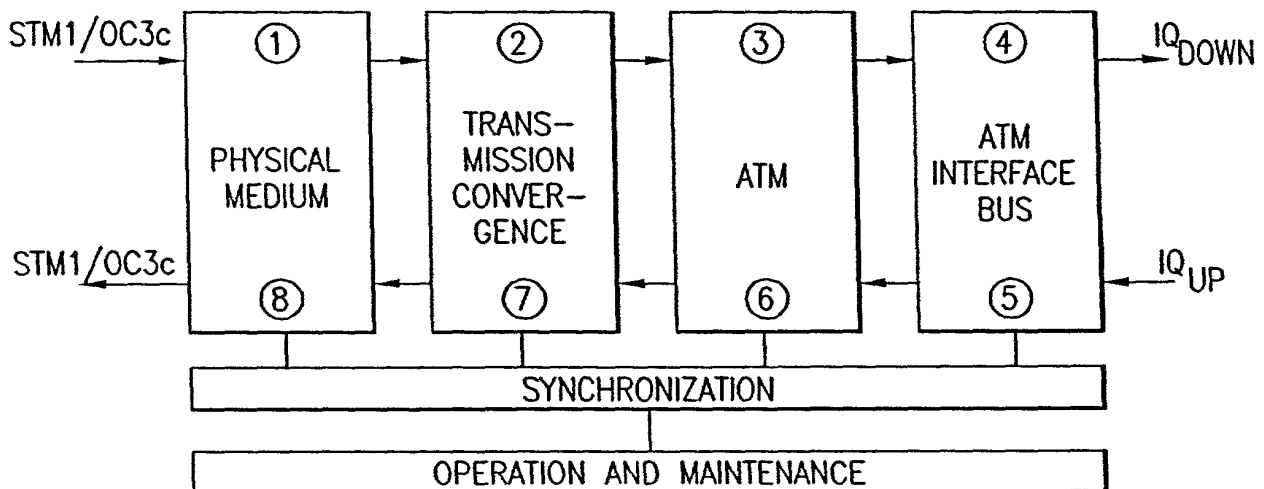


FIG. 14C

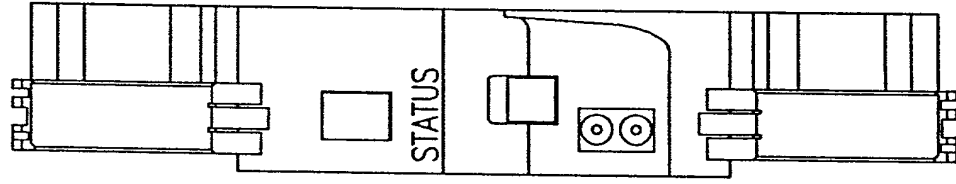


FIG. 14D

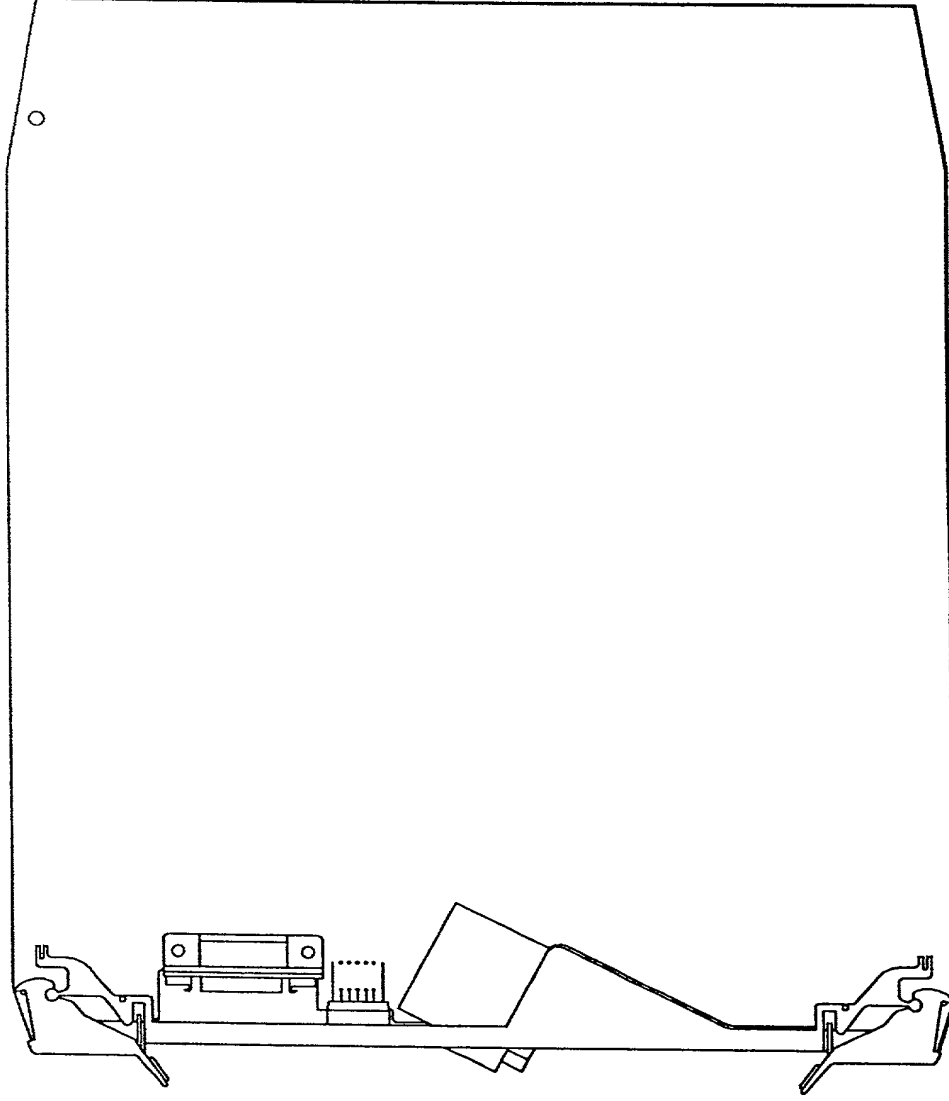


FIG. 14E

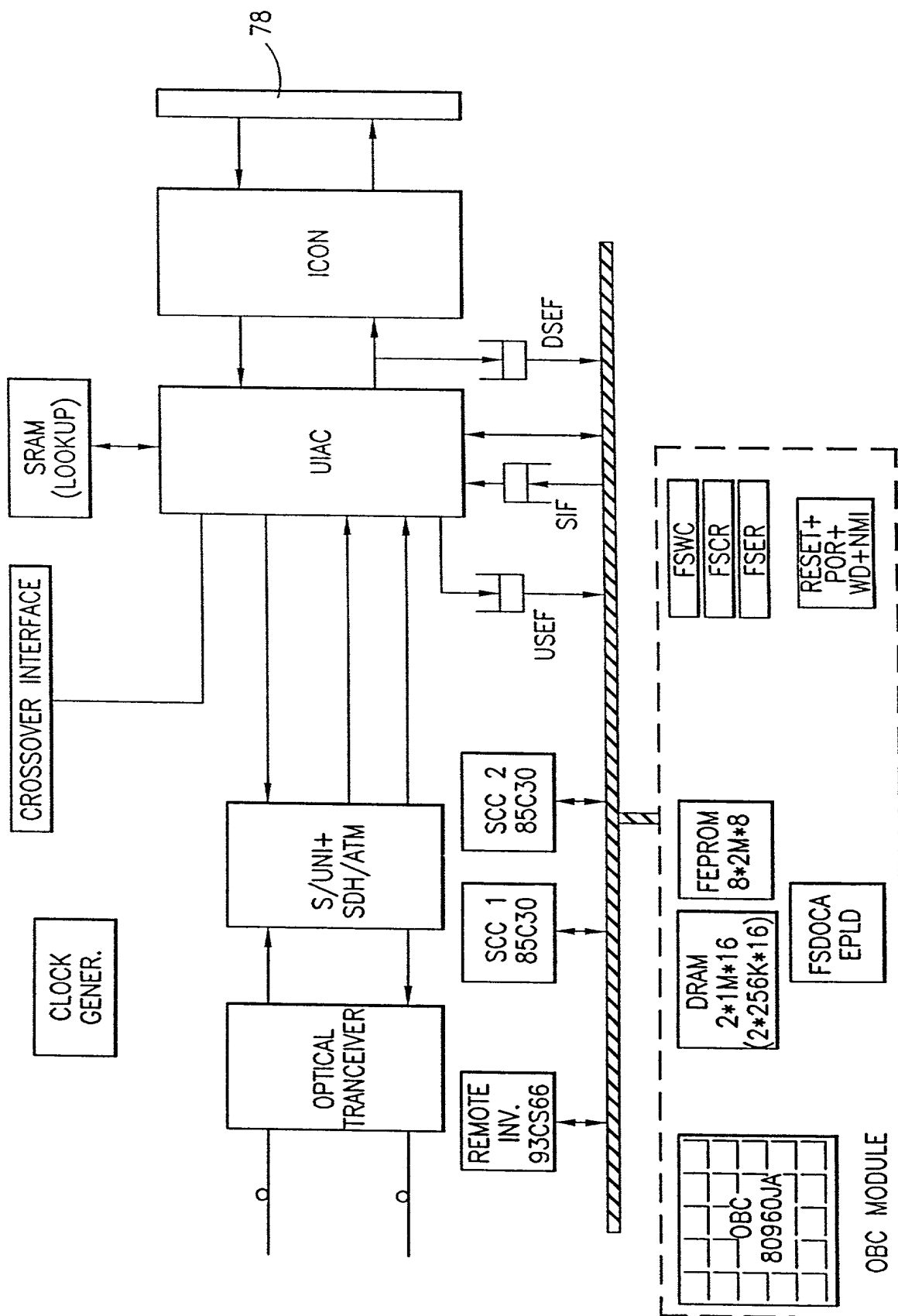


FIG. 14F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | BIT/OCTET |
|--------|---|---|---|-----|---|-----|---|-----------|
| GFC(*) | | | | VPI | | | | 1 |
| VPI | | | | VCI | | | | 2 |
| VCI | | | | | | | | 3 |
| VCI | | | | PTI | | CLP | | 4 |
| HEC | | | | | | | | 5 |

FIG. 14G

| VPI | | | VCI | | | | MODE |
|-----|----|----|-----|----|----|----|-------|
| #3 | #2 | #1 | #4 | #3 | #2 | #1 | |
| X | X | X | | | X | | NNI |
| | X | X | | | X | X | UNI 1 |
| | | X | | X | X | X | UNI 2 |

FIG. 14H

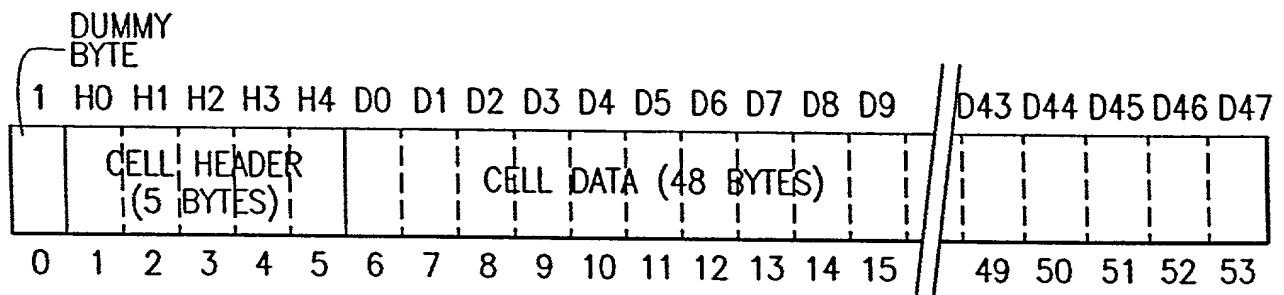


FIG. 15A

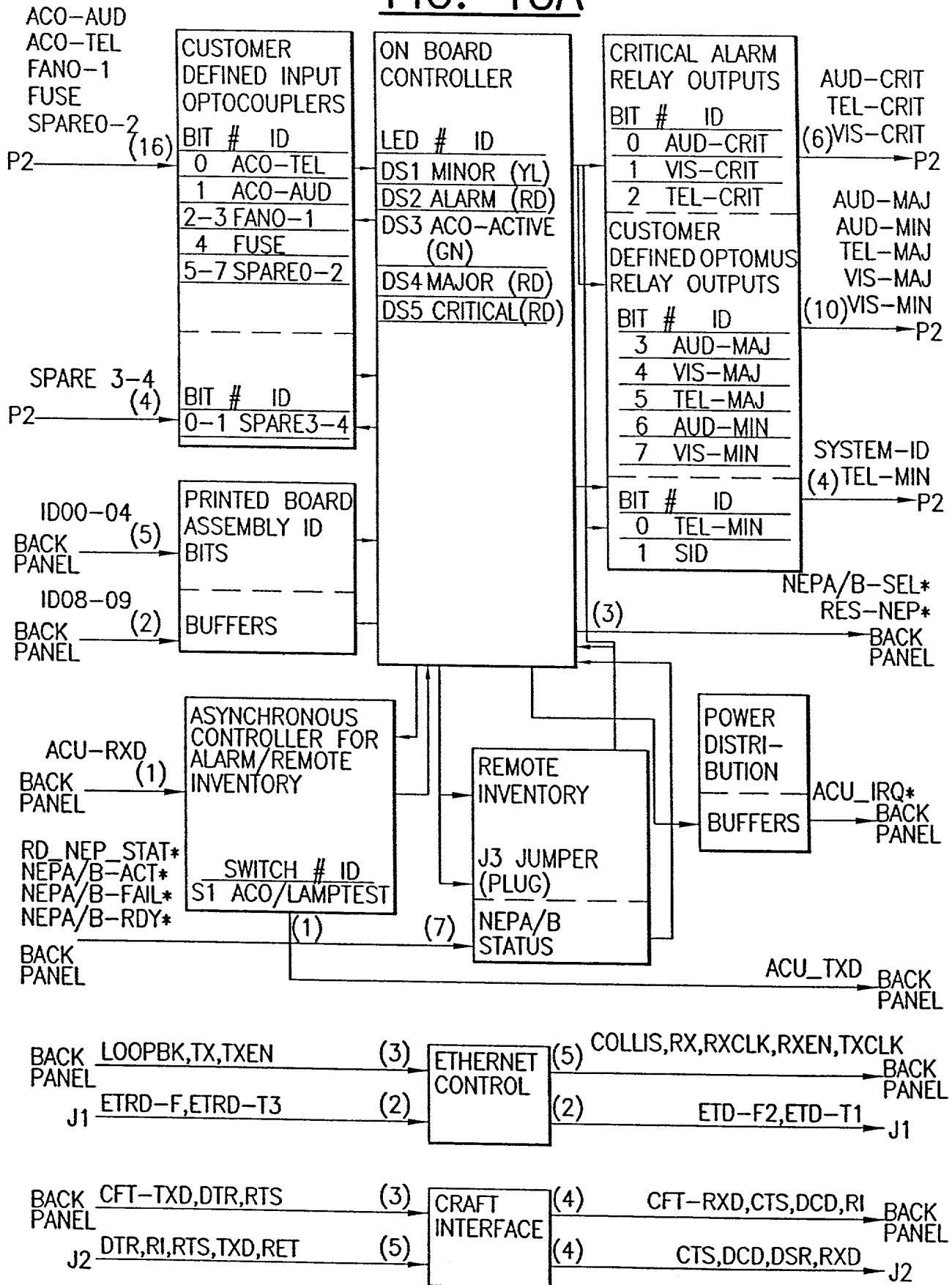


FIG. 15B

| Item Number | Function Description |
|-------------|---|
| 1 | Provides a central office alarm interface |
| 2 | Provides a telemetry alarm interface |
| 3 | Collects up to 2 rack fan alarms, 1 Top Rack Unit (TRU) fuse alarm, 5 miscellaneous external alarms, 1 Alarm Cut-Off Audible Unit (ACO_AU) alarm, and 1 ACO Telemetry (ACO_TEL) alarm |
| 4 | Provides local craft terminal port |
| 5 | Provides an ethernet port (future option) |
| 6 | Provides a visual summary alarm display of rack minor, major, and critical alarm conditions |
| 7 | Provides a local Alarm Cut-Off (ACO) for Central Office (CO) alarms and a visual display of the ACO status |
| 8 | Provides a unit failure indicator |
| 9 | Provides a craft port for an asynchronous EIA-232-D function available to the user via a female 9-pin subminiature D connector on the front panel of the ACU |
| 10 | Handles input/output alarm information and generates alarm status/indicators via relay contacts or optical switches and Light Emitting Diodes (LEDs) for audible/visual/telemetry |
| 11 | Provides for a remote inventory function |
| 12 | Provides for Network Element Processor A (NEPA)/NEPB active/standby arbitration (future option) |
| 13 | Provides for NEPA/NEPB reset function (future option) |
| 14 | Provides for Joint Test Access Group (JTAG)/boundary scan testing |

Note There is only one active craft port per ADSL system.

Note The backplane has 5 Identifier (ID) bits dedicated for slot information that are read to check for proper slot insertion (ie., each slot has a unique address).

FIG. 16

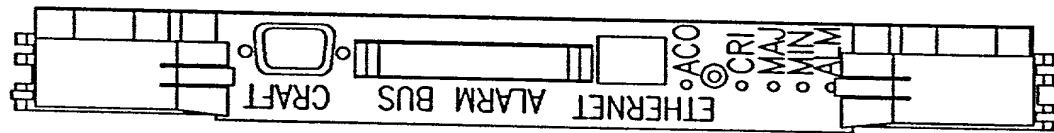


FIG. 17

